United States Patent

[11] 3,623,009

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[54] **ELECTRONIC PRINTING CALCULATOR**
20 Claims, 10 Drawing Figs.

[52] **U.S. Cl.** **340/172.5**
[51] **Int. Cl.** **G06f 3/00**
[50] **Field of Search** 340/172.5; 235/156

[56] **References Cited**

UNITED STATES PATENTS

3,074,635	1/1963	Borne et al.	235/156
3,460.095	8/1969	Caroussos	340/172.5
3,495,221	2/1970	Herendeen	340/172.5

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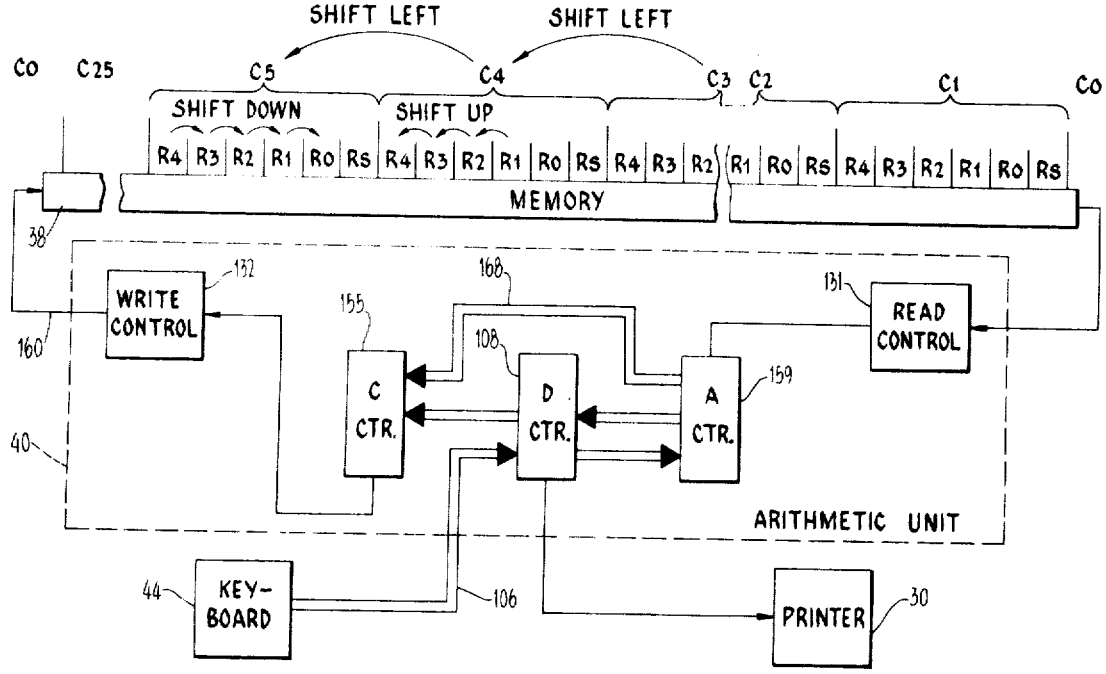
ABSTRACT: A desk-type calculator having a set of decimal digit keys, a decimal point key, a decimal point-setting switch, a set of function-initiating keys, a printing means, and electronic control means. A number, which may include either or both a whole portion and a decimal fraction portion, is entered into a memory means by operation of the digit keys and/or the decimal point key. Operation of a function key causes the number to be printed on a paper strip. The entered numbers are printed so that the least significant actually entered digits occupy the rightmost print positions; the decimal points are not intentionally aligned vertically. Upon execution of the operation commanded by the function key, such as, for example, addition, multiplication, division, etc., the result, or answer, is automatically printed on paper strip with the decimal point appearing at a location determined by the setting of the decimal point wheel.



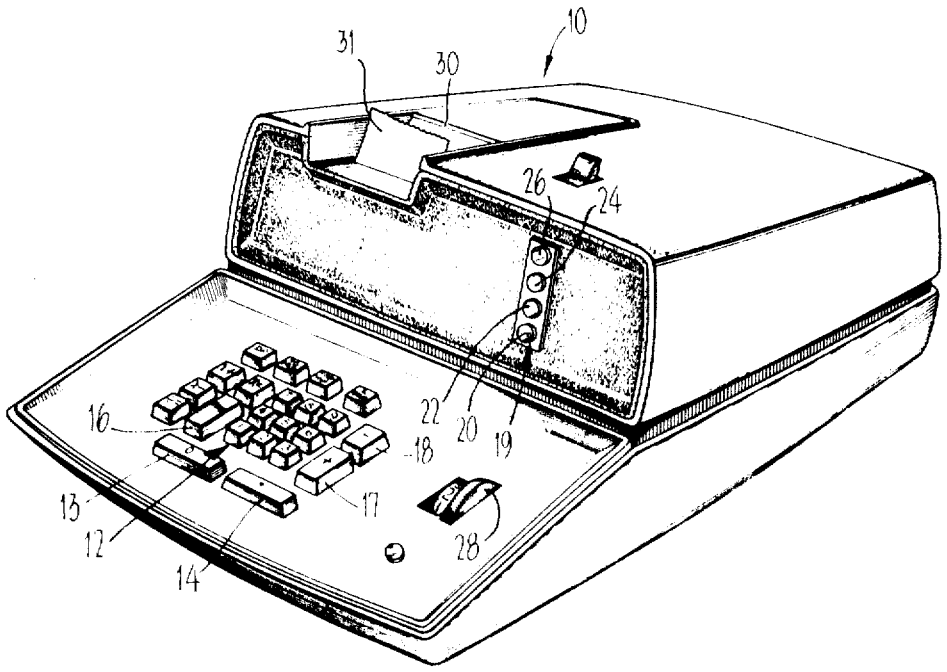


Fig. 1

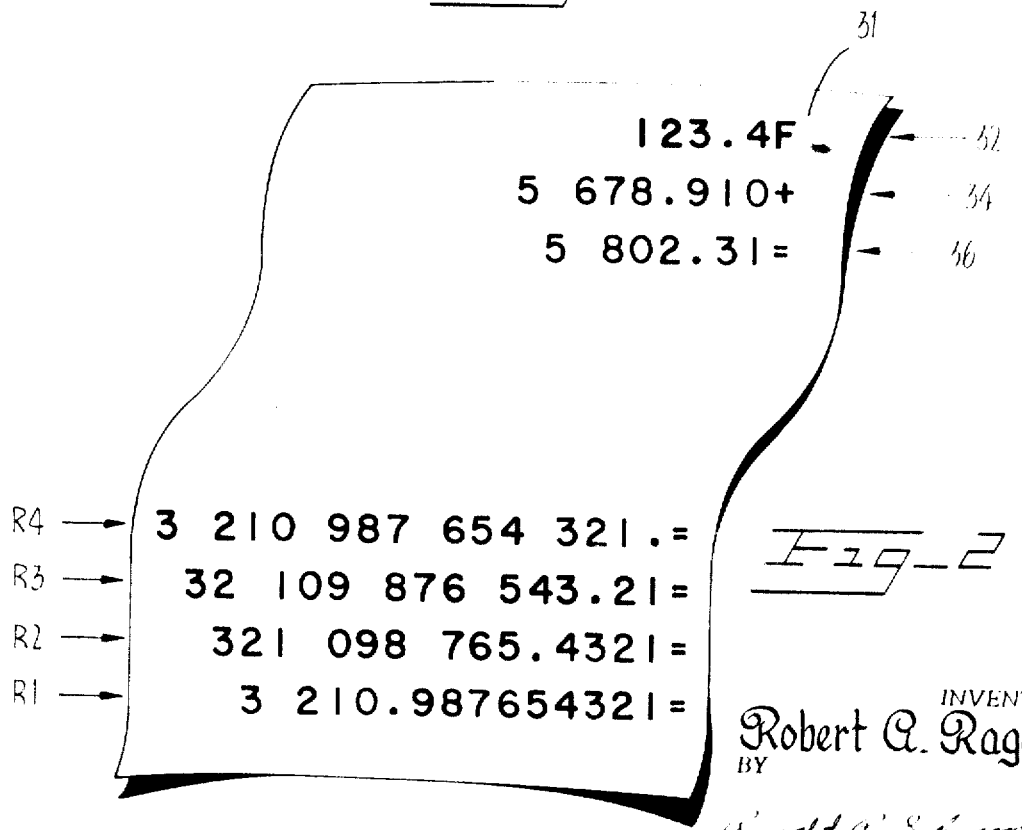


Fig. 2

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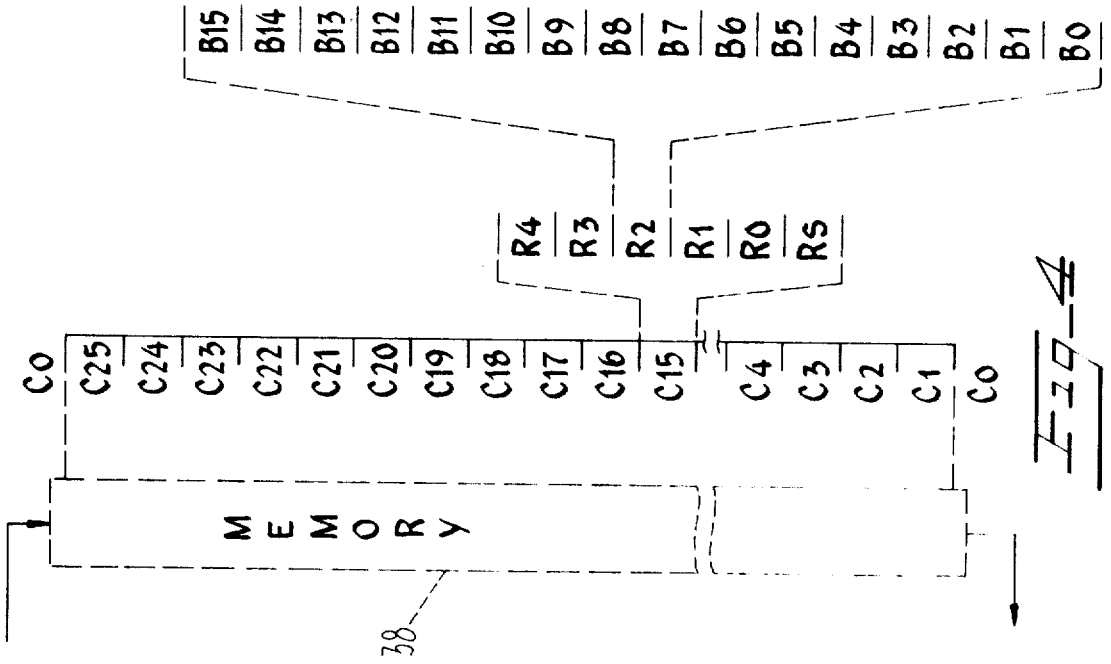
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
R4 R3 R2 R1 R0 R5
C0 C25 C24 C23 C22 C21 C20 C19 C18 C17 C16 C15 C4 C3 C2 C1 C0
MEMORY
38

Fig. 4

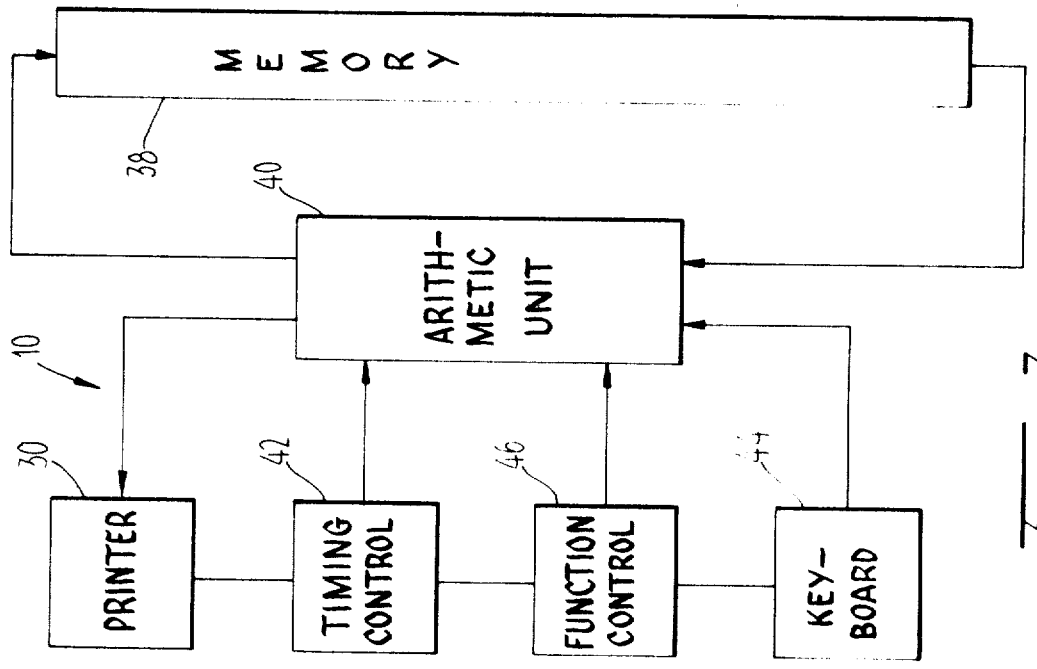
MEMORY
38
40
ARITH-METIC UNIT
10
30
PRINTER
42
TIMING CONTROL
46
FUNCTION CONTROL
KEY-BOARD

Fig. 3

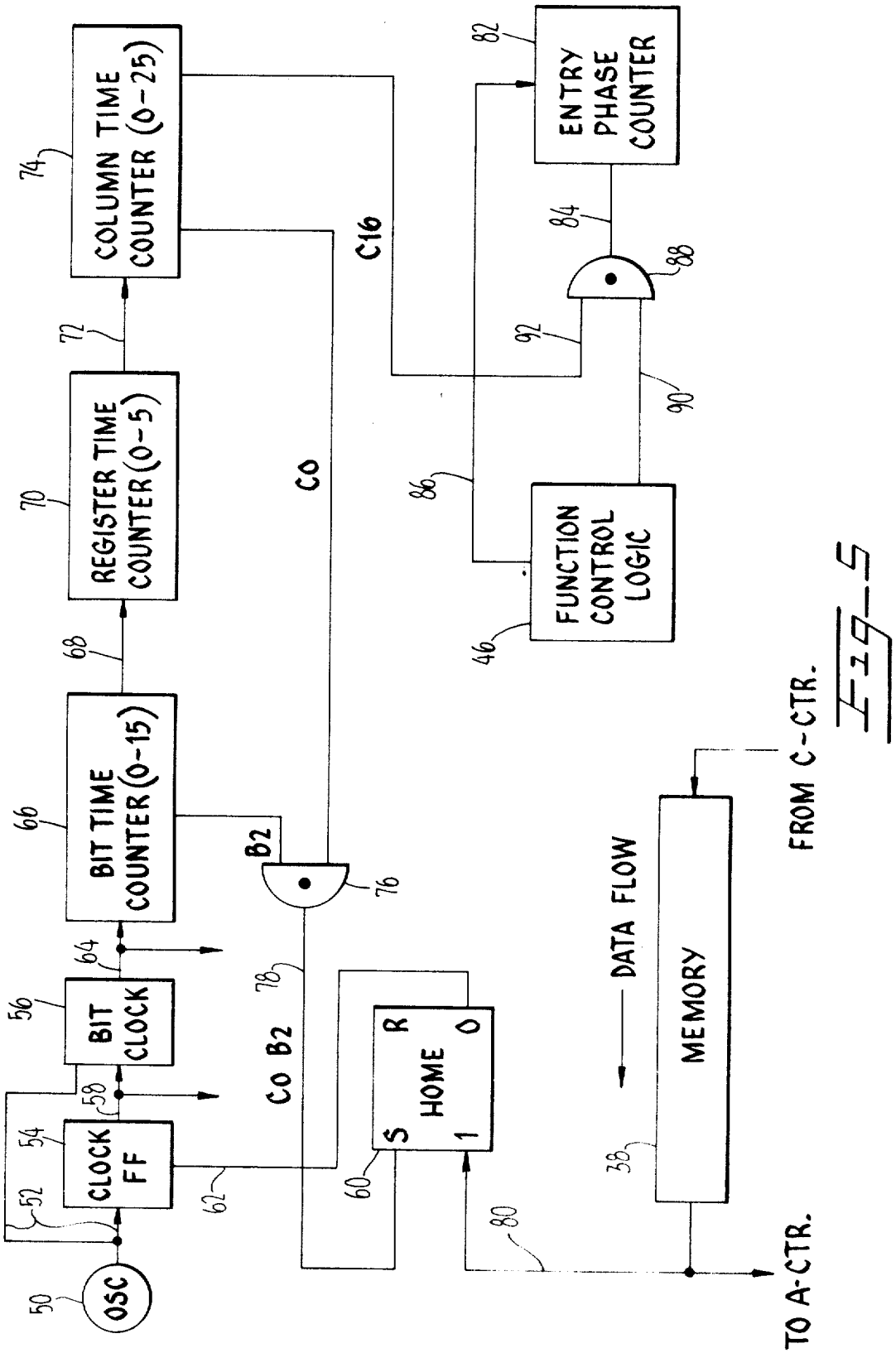
OSC
50
CLOCK FF
52
54
BIT CLOCK
56
58
64
BIT TIME COUNTER (0-15)
66
REGISTER TIME COUNTER (0-5)
70
68
COLUMN TIME COUNTER (0-25)
74
72
C16
C0
B2
76
78
C0 B2
62
S
R
HOME
1
0
60
80
ENTRY PHASE COUNTER
82
84
88
92
90
FUNCTION CONTROL LOGIC
86
46
DATA FLOW
MEMORY
38
FROM C-CTR.
TO A-CTR.

FIG. 5

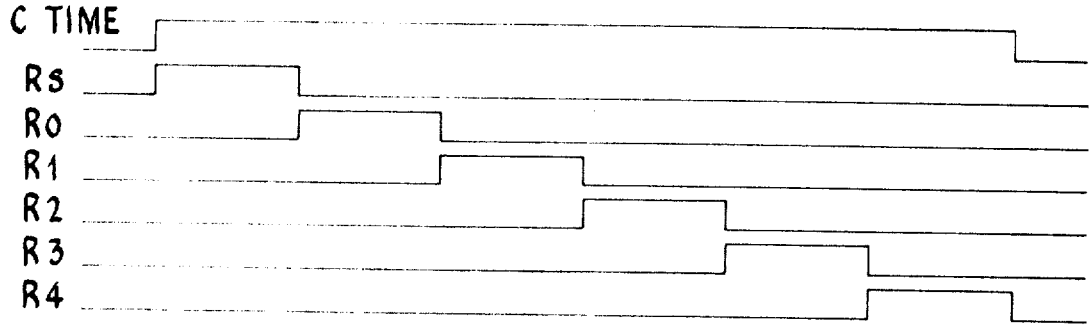
C TIME
Rs
R0
R1
R2
R3
R4

Fig_7

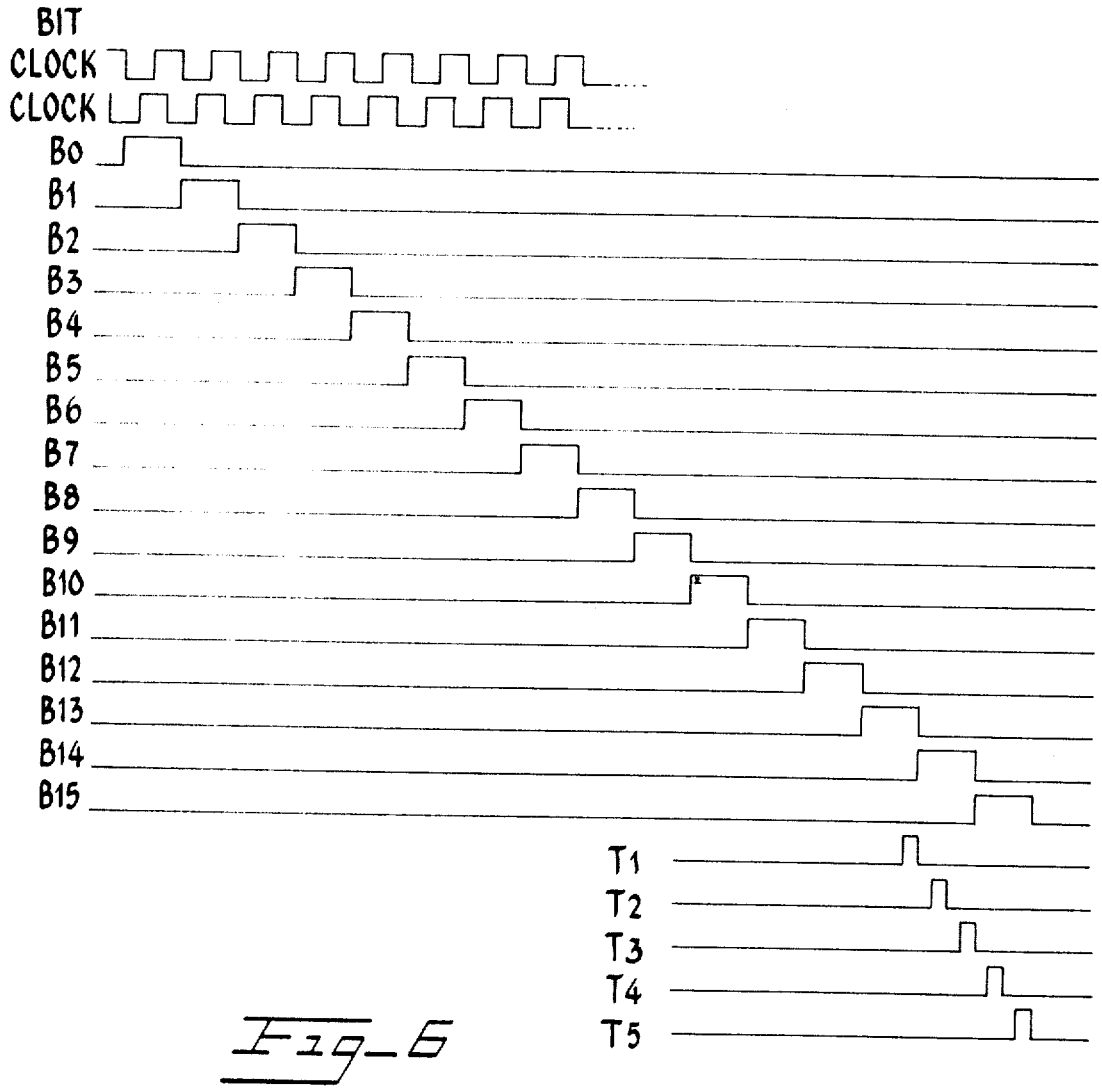
BIT
CLOCK
CLOCK
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
T1
T2
T3
T4
T5

Fig_6

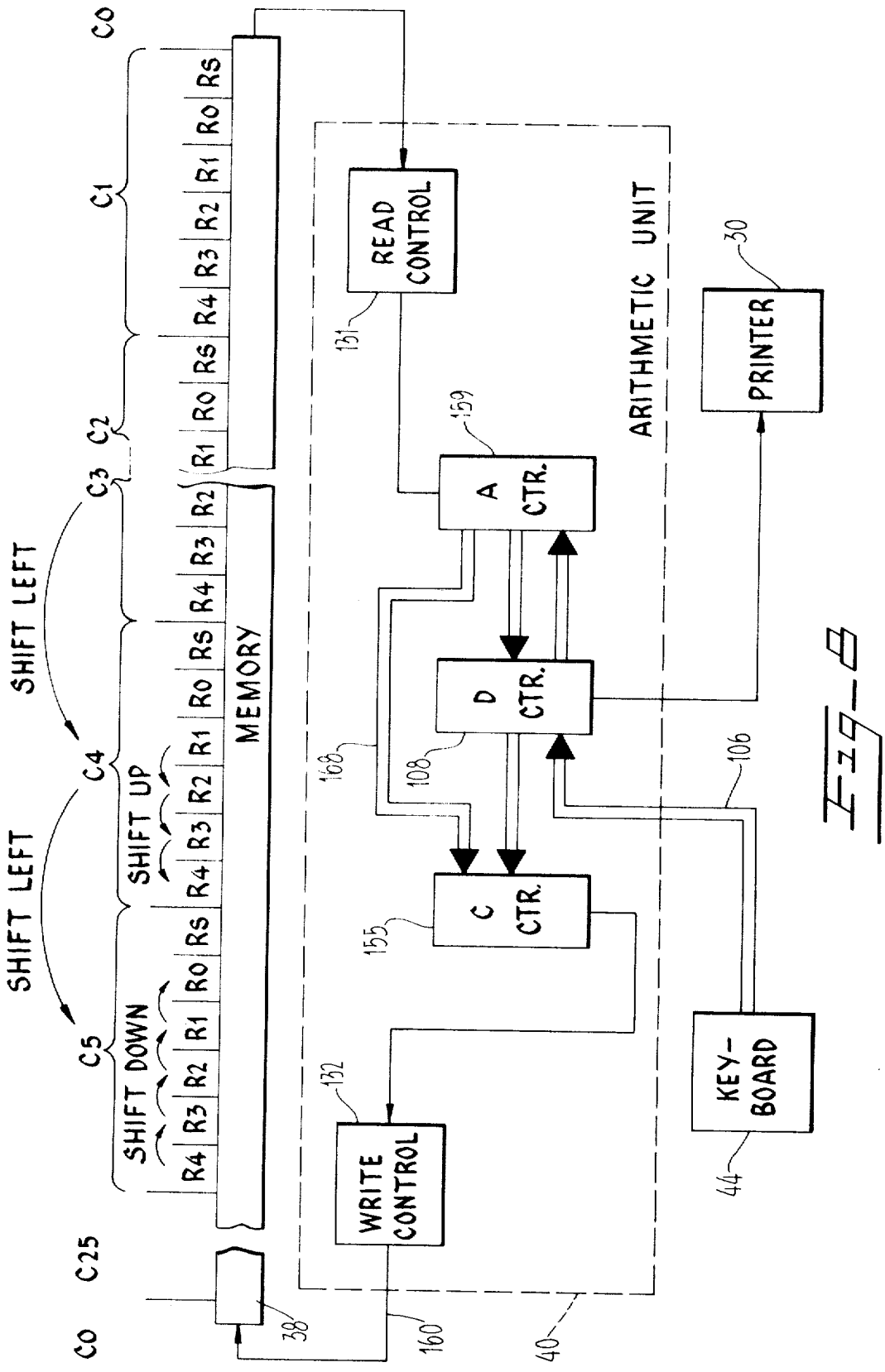
C0
C1
C2
C3
C4
C5
C25
C0
R0 R1 R2 R3 R4 R5
MEMORY
SHIFT LEFT
SHIFT LEFT
SHIFT UP
SHIFT DOWN
READ CONTROL
WRITE CONTROL
A CTR.
D CTR.
C CTR.
ARITHMETIC UNIT
PRINTER
KEY-BOARD
131
132
155
159
168
108
106
44
38
160
40
30

Fig-8

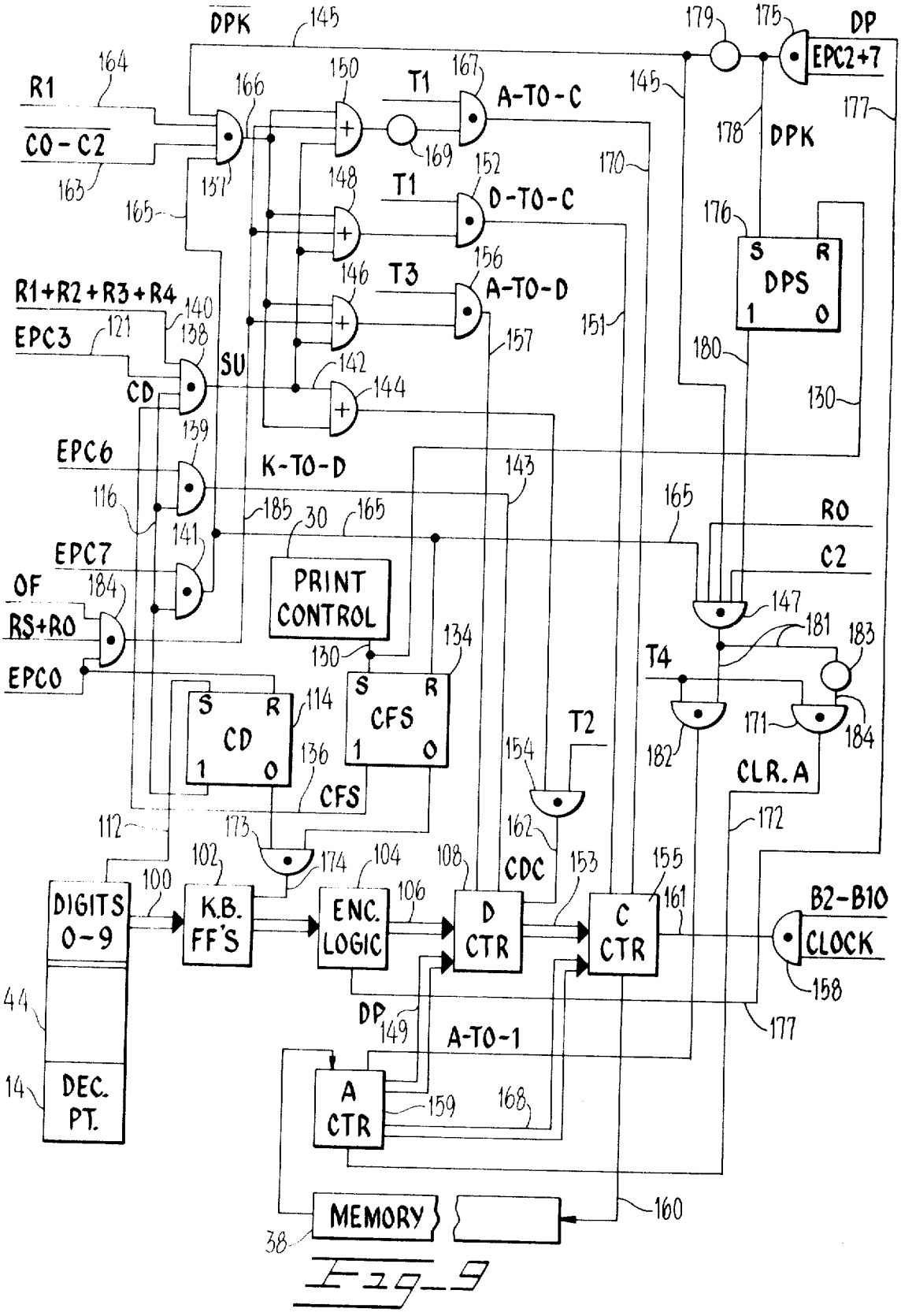
DPK
145
R1
164
CO-C2
163
166
150
T1
167
A-TO-C
169
151
148
T1
152
D-TO-C
165
146
T3
156
A-TO-D
157
R1+R2+R3+R4
140
EPC3
121
138
SU
CD
142
144
139
EPC6
K-TO-D
143
116
185
30
165
141
EPC7
OF
184
RS+RO
EPC0
PRINT CONTROL
130
134
S R
CD
1 0
114
S R
CFS
1 0
136
CFS
112
173
174
102
104
108
100
106
DIGITS 0-9
K.B. FF'S
ENC. LOGIC
D CTR
CDC
153
154
T2
162
C CTR
155
161
44
14
DEC. PT.
DP
149
A-TO-1
A CTR
159
168
MEMORY
38
160
177
179
175
DP
EPC2+7
145
178
DPK
170
176
S R
DPS
1 0
180
151
130
165
RO
C2
147
181
183
T4
171
184
182
CLR.A
172
B2-B10
CLOCK
158

Fig. 9

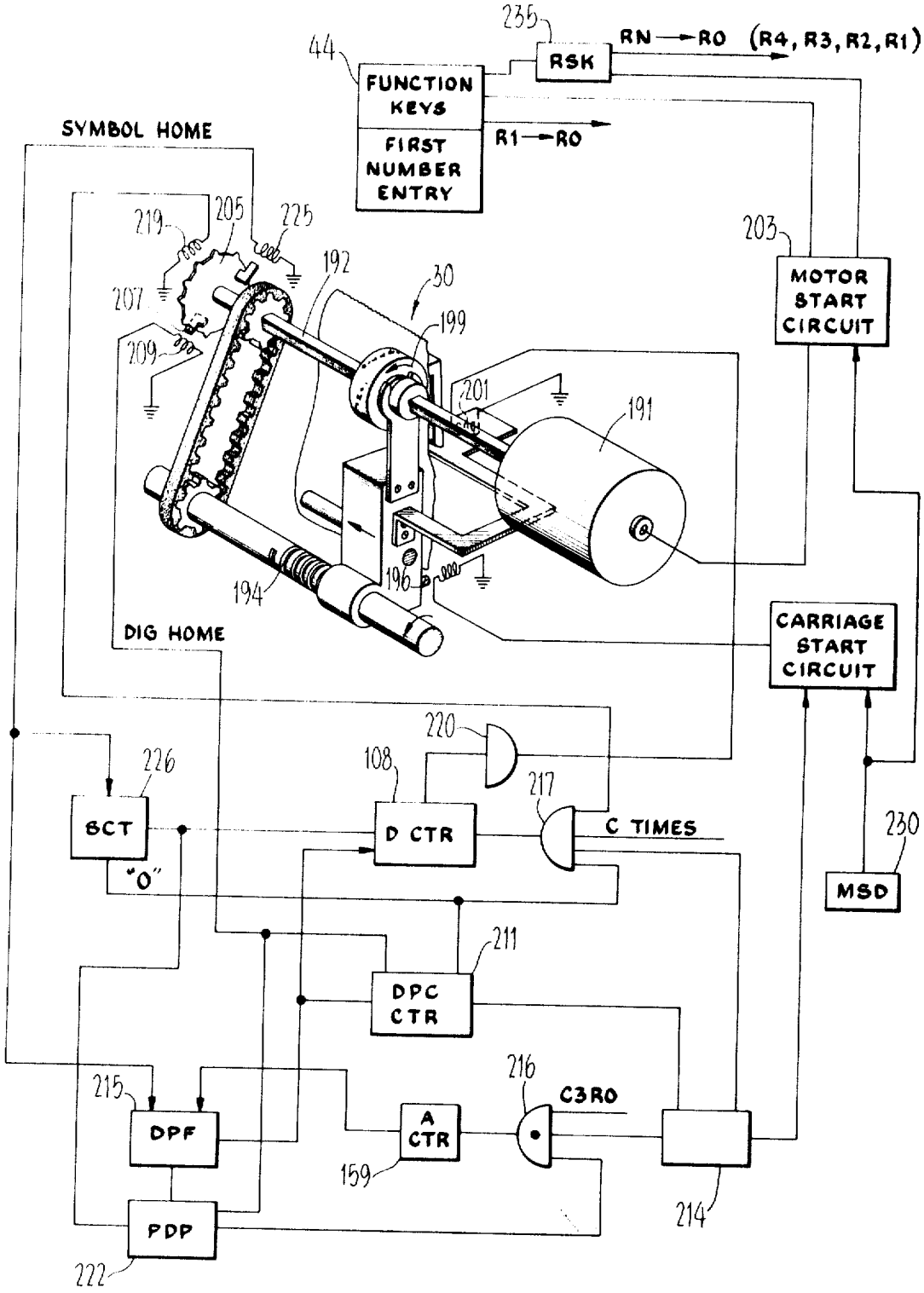
235
RN → RO (R4, R3, R2, R1)
RSK
44
FUNCTION KEYS
FIRST NUMBER ENTRY
R1 → RO
SYMBOL HOME
219
205
225
207
209
192
30
199
201
191
194
196
203
MOTOR START CIRCUIT
CARRIAGE START CIRCUIT
DIG HOME
220
108
217
C TIMES
226
SCT
"0"
D CTR
230
MSD
211
DPC CTR
215
DPF
216
C3RO
A CTR
159
214
PDP
222

Fig_10

ELECTRONIC PRINTING CALCULATOR

BACKGROUND

1. Field of Invention

This invention concerns a data-handling apparatus and more particularly pertains to a printing calculator for printing entered numbers in a natural or floating decimal point mode and for printing results of calculations in a predetermined fixed decimal point mode.

2. Prior Art

Throughout this application, the term "fixed decimal point" refers to the arrangement of digits and decimal point in a number wherein the location of the decimal point occurs at a predetermined location according to the setting of a switch, a thumbwheel, or other means on a calculator. If the decimal point switch is set at 2, the decimal point will always appear between the third and second rightmost digit positions on printout of the number or visual display of the number. For example, if the number 25 is entered, the printout will appear as 25.00. On the other hand, if the number 25.463 is entered, the printout will appear as 25.46; it will be noted that the least significant digit (3) has been truncated or lost.

The term "natural or floating decimal point" used in this application refers to an arrangement of digits and a decimal point in a number wherein the location of a decimal point occurs at a location determined by the natural entry of the number into a calculator. For example, if the number 25 is entered, the printout will appear as 25, while if the number 25.463 is entered, the printout will appear as 25.463.

Some prior art calculators of the mechanical and/or electronic type having what is termed a 10-key keyboard for sequential entry of the separate digits of a number include a switch or thumbwheel for presetting the location where a decimal point is to appear in the entered numbers and in the result of arithmetic operations on those numbers. Certain advantages are found with the use of such a preset or fixed decimal point. In adding a series of numbers with such a calculator, it is usually necessary to set the decimal point switch so as to accommodate a number having the most number of digits in a decimal fraction portion. For example, in adding a series of numbers, it is usually required that the numbers be entered manually into the calculator in such a manner that the decimal points of all the numbers be aligned so that the operation of addition may be performed correctly. The automatic decimal point-setting wheel must be preset to handle a number having the greatest expected quantity of decimal fraction portion digits. Thus, for example, if a series of numbers are to be added, any one of which could have up to four decimal fraction digits (digits to the right of a decimal point) the decimal point setting switch must be set to 4. Now, when a number having less than four decimal fraction digits is entered, the internal logic will provide automatically additional zeros to the rightmost positions of the decimal fraction portion so that the decimal point will occur in printout or visual display in the proper place. Assume, as an example, that the decimal point switch is set at 4, and the number entered by manual operation of the digit keys and decimal point key is 12.3, the printout will appear as 12.3000. Likewise, the number 12.34 entered manually will appear on printout as 12.3400; addition of the two numbers will cause a printout of 24.6400. On the other hand, entry of the number 12.34563 will cause a printout of 12.3456; the fifth or least significant digit (LSD) of the entered number has been dropped or ignored. This is satisfactory if such least significant digit is not important.

However, if it is desired to maintain a printed record or have a visual display of all the digits entered, even though some of the lowermost significant digits are not utilized in the operations or calculations performed on the number, it can be readily appreciated that some other provision must be made. Thus, while the aforesaid prior art decimal point switch is useful and advantageous, there is need, in a calculator, for providing control of printout of decimal fraction portion digits in both an entered number and the results of arithmetic operations on the entered numbers.

SUMMARY

Therefore, in accordance with this invention, there is provided in an electronic calculator a control for limiting the answers of an arithmetic operation on numbers previously entered to a predetermined quantity of digits in the decimal fraction portion without, however, affecting any limitation (within the capacity of the machine) on the quantity of whole number digits that may be entered into the calculator having a capacity of 13 digits. Or, it may be desired to add a series of numbers having four digits in the decimal fraction portion but to have a sum having only two digits in the decimal fraction portion.

It is, therefore, an object of the present invention to provide an improved electronic calculator of the printing type.

The features of novelty that are considered characteristic of this invention are set forth with particularity in the appended claims. The organization and method of operation of the invention may best be understood from the following description when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a calculator incorporating the principles of the present invention.

FIG. 2 is an illustration of the printout accomplished with the calculator of FIG. 1.

FIG. 3 is a simplified block diagram of the calculator of FIG. 1.

FIG. 4 is a chart showing the organization of data in the memory means of FIG. 3.

FIG. 5 is a simplified logic diagram showing the timing control for the present invention.

FIG. 6 is a timing diagram illustrating the bit times generated by the timing control of FIG. 5.

FIG. 7 is a timing diagram illustrating the register times generated by the timing control of FIG. 5.

FIG. 8 is a simplified block diagram showing the major operational unit's organization of the calculator incorporating the present invention.

FIG. 9 is a logic diagram illustrating various control features of the present invention.

FIG. 10 is a logic diagram illustrating the printing control of the present invention.

FIG. 10 is a logic diagram illustrating the printing control of the present invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

One preferred embodiment of the present invention will now be described with reference to the drawings in which like reference characters refer to the same parts throughout the different figures.

In FIG. 1 there is shown a calculator **10** of the printing type, having a set of 10 digit or numeral keys **12**, including a zero or naught key **13**, a decimal point key **14**, a set of function keys, such as Enter key **16**, Add key **17**, Subtract key **18**, etc., a battery or array **19** of four register contents indicating lamps **20**, **22**, **24**, and **26**, a decimal point setting switch **28**, and a printing unit **30**.

In FIG. 2 there is shown a typical printout on paper **31** of an augend **32**, an addend **34**, and their sum **36** according to the present invention. As seen in FIG. 2, augend **32**, is a number having three whole portion digits (numerals to the left of the decimal point) and one decimal fraction portion digit (numerals to the right of the decimal point). The letter F to the right of the number 4 in the augend **32** indicates that the number was entered by operation of Enter key **16**. THe addend **34** is a number having four whole portion digits and three decimal fraction portion digits. The symbol + to the right of the numeral 0 in the addend **34** indicates that the number was entered by operation of Add key **17**.

It is to be noted that the rightmost digit of the addend **34** is a zero or naught; this results from the aught key **13** having been the third digit key depressed after the decimal point key **14** had been depressed when the addend **34** was entered into the calculator. It is shown in FIG. **2** that the augend **32** contains only one decimal fraction portion digit; this resulted from depressing only one digit key (the digit key for numeral 4 after depression of the decimal point key **14** when the augend **32** was entered into the calculator. FIG. **2** thus demonstrates one feature of the present invention, namely that the numbers entered into the calculator appear, on printout, in their natural order, i.e., the decimal point of the entered numbers does not appear in a fixed location but appears in a "floating" or variable location according to how many digit keys **12** are actuated after the decimal point key **14** is actuated.

In FIG. **2** there is also shown the printed result or sum **36** of the addition of addend **34** to augend **32**. It is shown that the sum **36** has two digits in its decimal fraction portion. The number of digits appearing in the result of any function or operation on entered numbers is determined and controlled by decimal point switch **28** (FIG. **1**). As shown in FIG. **1**, the decimal point switch **28** is positioned to display the numeral 2. Thus, according to another feature of the present invention, the result of arithmetic operations on numbers previously entered into the calculator will be printed with as many decimal fraction digits as dictated or controlled by the decimal point switch **28** regardless of how many decimal fraction portion digits are in the numbers entered into the calculator.

In addition, it is seen in FIG. **2** that the numbers to the left of the decimal point are printed in groups of three, i.e., there is a space between each group of three characters. This provides the advantage of easy readability of multidigit whole portion numbers.

In FIG. **3** there is illustrated, in block diagram form, the major functional or operational units comprising one embodiment of the calculator **10** of FIG. **1**. The calculator **10** includes a dynamic memory or storage means **38** interconnected with an arithmetic unit **40** to form a recirculating data or memory loop. A timing control unit or means **42** is interconnected with other units of the calculator to synchronize the flow of data and control signals between the memory and the other functional units. A keyboard unit **44**, which contains the digit keys **12**, naught key **13**, decimal point key **14**, decimal point switch **28**, and function control keys as shown in FIG. **1** is connected with a function control unit **46** and the arithmetic unit **40**. The printer **30** is connected between the timing control unit **42** and arithmetic unit **40** for printout of numbers entered into the calculator and results of arithmetic operations on the numbers so entered.

Only those details of the functional units of FIG. **3** that are necessary to an understanding of the present invention are set forth in this application.

The memory **38** in the illustrated embodiment of the present invention comprises a dynamic memory of the type commonly known as an ultrasonic or magnetostrictive delay line through which information or data is represented by and caused to travel in the form of a train of mechanical disturbances commonly termed acoustic pulses. Other types of memory means **38**, either static or dynamic, such as for example, a magnetic drum or disc, may be utilized as will readily occur to those skilled in the art to which the present invention pertains. The acoustic pulses are entered or launched serially into the memory **38** from the arithmetic unit, take a predetermined time to travel the length of the memory, and then are entered back into the arithmetic unit; this is termed a data loop.

Each number entered from the keyboard **44** by operation of the digit keys is converted or transformed into a series or set of pulses traveling serially through the data loop. Briefly described, a digit of a number (which number may include a whole portion and decimal fraction portion) is represented, in the memory **38**, by a set of pulses, the number of pulses being equal to the ordinal value of the digit. Thus, for example, the digit or numeral 4 is represented by a set of four pulses, while the digit or numeral 7 is represented by a set of seven pulses. It can be understood that digits or numerals having different ordinal values will be represented by different sets of pulses. This is termed a pulse-count system of notation.

For the purpose of verbally describing this invention, the binary symbol "1" is representative of a pulse in the memory **38** at a particular space-time unit, or pulse-time, hereinafter termed bit-time, while the binary symbol "0" is representative of the lack of a pulse at a particular bit-time in the memory. Assume that the amount of bit-times in the memory required to hold the absolute value of a digit is equal to nine. It can be understood that the decimal digit 4 would appear in the memory **38** as

0 0 0 0 0 1 1 1 1

while the decimal digit 7 would appear as

0 0 1 1 1 1 1 1 1

Thus, the number 47 would appear as

0 0 0 0 0 1 1 1 1 0 0 1 1 1 1 1 1 1

From the above, it can be understood that each single decimal digit of a number requires a fixed number of bit-times in the memory **38**.

The organization of the data or space-time compartments in the memory **38** will now be described with reference to FIG. **4**. The memory **38** may be considered to be divided into 25 equal space-time compartments termed column-times or C-times and labeled **C1** through **C25**. It is to be noted that in FIG. **4** there is also indicated a CO-time, the length (space-time) of which is somewhat indefinite, but may be said to be the space or time between the occurrence of a last C-time (**C25**) and the occurrence of the next succeeding first C-time (**C1**).

Each C-time is subdivided into six register or R-times of equal space-time length. For example, in FIG. **4** there is shown that **C15** is subdivided into RS, RO, **R1**, **R2**, **R3**, and **R4**-times. It will be understood that each of the other C-times (except CO) are also subdivided into similar equal length (space-time) RS, RO, **R1**, **R2**, **R3**, and **R4**-times. The set of the 25 RS-times comprise a special storage register, the use of which is not germane to the present invention. The set of 25 RO-times comprise a special register termed RO register used internally by the calculator as will be described later. The other four sets of register times comprise internal storage registers, the first (**R1**) and second (**R2**) of which will be described in more complete detail as the description proceeds.

Each register time or R-time is further subdivided into 16 bit-times or B-times as illustrated in FIG. **4** with respect to **R2C15**. Each bit-time is the space-time required for occupancy of one acoustic pulse or binary 1 in the memory **38**. In general, a maximum of only nine bit-times in each set of 16 bit-times are utilized to represent a decimal digit's ordinal value, according to the pulse-count system of notation mentioned previously.

A single internal register, within the meaning of that term as used herein, may be considered to be formed by a set of 25 successive RN-times (where N represents S, O, 1, 2, 3, or 4).

In the lower half of the strip of paper **31**, shown in FIG. **2**, there is illustrated the printout of typical contents of each of the four registers **R1**, **R2**, **R3**, and **R4**. It is to be noted that each register's printout contains 13 digits (the maximum possible). The number in **R4** is a whole number and has no decimal fraction portion. Thus, the least significant digit (the numeral 1) of the number in **R4** is the digit immediately to the left of the decimal point. The other three registers (**R3**, **R2**, and **R1**) contain numbers having decimal fraction portions. Those numbers that contain a decimal fraction portion have their least significant digit at the extreme rightmost portion of the printed number and, of course, such location is to the right of their decimal points. It should be kept in mind that if the aught digit key **13** on the keyboard (FIG. **1**) is the last digit key operated when entering a number having a decimal fraction portion a naught or 0 will appear in the number's printout as the number's least significant digit. Such a number having an aught as a least significant digit is shown in the upper portion of the paper strip **31** of FIG. **2** as previously mentioned addend **34**.

Each particular digit of a number entered into a particular register occupies the associated R-time of a particular C-time in the memory. In the preferred embodiment, the least significant digit of a number in a register occupies the associated R-time of C3-time, the next least significant digit occupies the associated R-time of C4-time, etc. Thus, the least significant digit 1 of R1 (as shown in FIG. 2) occupies the R1-time of C3-time shown in FIG. 2; the least significant digit 1 of R2 (as shown in FIG. 2) occupies the R2-time of C3-time shown in FIG. 5, etc.

The C1 and C2-times are reserved for other uses as will be described below. It can thus be understood that the internal registers (RS, RO, R1, R2, R3, and R4) of the calculator of the present invention are comprised of serially interspersed or interlaced compartments (R-times) according to a regular sequence, and the digits of a number in any one or more internal registers occupy interspersed space-time compartments (C-times) according to a regular order.

The arrangement of digits of a number (or as is sometimes called "data word") as just described, is not an invariable arrangement. The foregoing described arrangement is to be kept in mind, however, as a reference point in the discussion of shifting operations on the digits according to the present invention, to be described hereinafter.

According to one feature of the present invention, a first number having up to 13 digits is entered into register R1 from the keyboard. Each digit of the number, when entered, occupies the R1-times of column-times C3 up to C16. If the number includes a decimal fraction portion, the quantity of digits or numerals in such decimal fraction portion is recorded in the C2R1-time. For example, if the first number entered into the calculator contains nine digits in its decimal fraction portion (as shown in FIG. 2 for the printout of R1), there will be recorded a "9" in C2R1-time. The recording of decimal fraction digits is accomplished by counting the number of times the digit keys are operated subsequent to operation of the decimal point key 14.

According to another feature of the invention, after a number is entered, and an arithmetic function key, such as for example, Add key 17 is operated, shifting of the contents of internal registers R1 and R2 to the left as many digit positions as required to have the least significant digit of the whole number portion in the respective C12R1-time and C12R2-time. This, of course, will place the most significant digit of the decimal fraction portions (if the number contains a decimal fraction portion) in C11R1-time and C11R2-time, respectively. It can thus be understood that a number having 13 digits in its whole number portion (such a number is shown in FIG. 2 as the printout for R4) will be contained in the associated R-times associated with C12 through C24-times. On the other hand, a number having only four whole portion digits (such as the number shown in FIG. 2 as the printout for R1) will be contained in the R-times associated with C15 through C3-times. It is to be noted that since the number shown in FIG. 2 as the printout for R1 contains nine decimal portion digits when first entered, the least significant digit of the whole number portion is automatically placed in the C12R1-time position when the number is first entered and thus will have no left shift performed on it.

It can thus be understood that from zero to nine digit shifts will be required to shift an entered number so that the least significant digit of its whole number portion will be placed in C12R1-time, depending on how many decimal faction portion digits are part of the entered number. The quantity recorded in C2R1-time (which, it will be recalled, is equal to how many digits are in the decimal fraction portion of the entered number) is used to control the number of left-digit shifts. It should be clear that the number of left-digit shifts is equal to nine minus the quantity of decimal fraction digits in the entered number.

According to the present invention, the number of decimal fraction portion digits as recorded or stored in C2R1-time is utilized to control the printing of the number in register R1. This is accomplished according to the present invention by appropriate shifting operations as will be described in more detail hereinafter.

It can be understood from the above that the two numbers now in registers R1 and R2 are effectively, decimally aligned, that is, the least significant digit of their whole number portions each occupy C12-time of the associated R2 and R1-times. It can thus be appreciated that arithmetic operations may now be performed readily without having to make special adjustments for misaligned "decimal points." If an arithmetic operation was called for by depression of an appropriate arithmetic key on the keyboard at the time of entering the second number, that arithmetic operation will now be performed. The results of the arithmetic operation will be automatically placed in register R1 and appropriately or automatically aligned around C12R1-time. If the arithmetic function performed was multiplied or divided, the product or quotient, respectively, will be automatically printed on paper tape. If the arithmetic function performed was an addition or subtraction, the sum or difference, respectively, is not automatically printed out at this time, but is merely held in register R1. The new contents of R1 may be considered to be simply a first-entered number and, accordingly, a second number may be entered into the calculator for appropriate operations in the same manner as described above. However, if as a result of an addition or subtraction operation it is desired to printout the sum or difference (number in R1), the Enter key 16 is actuated. This will initiate printout of such result or answer, such as for example, the sum 36 shown in FIG. 2. Printout of the answer resulting from any arithmetic operation will include only as many decimal fraction portion digits as determined by a previous setting of the decimal point setting switch 28 (FIG. 1), regardless of how many decimal fraction portion digits were contained in any of the numbers entered into the calculator for operation thereof, according to another feature of the present invention.

Further, printout at any time whether upon entry of a number or upon the answer derived by arithmetic operations is accompanied in a manner so as to divide the whole portion digits of the number into groups of three for ease in reading such number. For example, as shown in FIG. 2, the numbers shown as the printout for R4 contains four groups of three digits each, plus a fifth group of one digit (most significant, digit 3. The manner of accomplishing this separation into groups of three or less according to another feature of the present invention will be described in detail along with the detailed description herein below of the printing operations.

There will now be described in more particular detail the preferred embodiment of the present invention by means of what is generally known as logic diagrams. The logic elements shown and described herein to implement the present invention may comprise any well-known electronic (or mechanical, electromechanical, fluidic, etc., as desired) circuit for implementing the required logic function, such as for example, AND, OR, a shift register, a binary counter, an inverter, etc. The voltages and/or current values from a power supply to operate the various logic elements may be any predetermined value compatible with the circuits utilized. Throughout the remainder of this description, various logic element input and output pulses or signals will be designated true or 1-level, while other pulses or signals will be designated false or 0-levels; the actual values of such pulses or signals may be any predetermined value required for the logic element to properly perform its intended function.

In order to properly gate and synchronize information and data signals in the calculator, there is provided a source of regularly recurring timing signals.

The timing control unit 42 of FIG. 3 is shown in further detail in FIG. 5 and is described more fully herein. Means for generating regularly recurring sets of timing signals are well known in the art to which the present invention pertains. More complete details of the timing control unit are shown and described in U.S. patent application, Ser. No. 682,194, filed Nov. 13, 1967, by Carl E. Herendeen entitled "Data Detec-

tor" now U.S. Pat. No. 3,495,221 issued Feb. 10, 1970 and assigned to the same assignee as the present application.

Briefly described, a free-running oscillator **50** transmits a continuous train of alternate 1-level and 0-level pulses, via a lead **52**, to a Clock flip-flop **54** and a Bit Clock flip-flop **56**. The Bit Clock flip-flop is enabled by 1-level Clock signals from Clock flip-flop **54**, via a lead **58**, while the Clock flip-flop is enabled by a 1-level signal from a Home flip-flop **60** via a lead **62**. So long as the Clock flip-flop **54** is enabled, the oscillator's output pulses, which in one embodiment occurs at a rate of about 2.8 MHz., cause the Clock flip-flop to transmit a series of Clock Pulses (shown in timing diagram FIG. **6**) to the Bit-Clock **56**, and other parts of the calculator, at a rate of one-half the oscillator frequency. The Bit-Clock **56** will be caused to transmit a series of Bit Clock Pulses (shown in timing diagram FIG. **6**) over lead **64** at the same rate as the Clock pulses, but lagging by 90°.

A bit-time counter **66** receives and counts the incoming Bit Pulses on lead **64**. The bit-time counter may be any well-known binary or decade counter capable of counting from zero to 15 and returning to zero on the 16th count and then resuming the counting again. Each time the bit-time counter changes from a count of 15 to a count of zero (the 16th count), a Bit-Time Pulse is transmitted via a lead **68** to a register-time counter **70**. The register-time counter, like the previously mentioned bit-time counter **66**, may be any well-known binary or decade counter capable of counting from zero to five, returning to zero on the sixth count and proceeding to count up again. Each time the register-time counter changes from a count of five to a count of zero (the sixth count), a pulse is transmitted via a lead **72** to a column-time counter **74**.

The column-time counter **74** may be any well-known binary or decade counter capable of counting input pulses from zero to 25, returning to zero on the 26 pulse and proceeding to count pulses again.

Throughout the calculator **10** of the present invention, various logic gates and other logic elements are enabled and disabled at various times by appropriate leads connected between the element or gate and various stages of the bit-time counter **66**, the register-time counter **70**, and column-time counter **74**, in addition to the output leads from the Clock flip-flop **54** and Bit-Clock flip-flop **56**. In order to simplify the logic diagrams and the description, most of the decoding gates for detecting the various states or counts (timing signals) of the timing chain elements will not be shown; instead, short leads will be shown and marked with the appropriate timing signals. It will be understood that such leads or timing signals originate from appropriate gates suitably connected directly or indirectly with the elements of the timing chain just described.

Home flip-flop is placed in its set condition, thereby changing the signal on output lead **62** from 1-level to 0-level which thus disables the Clock flip-flop **54**. Disabling of the Clock flip-flop will inhibit transmission of any further Clock pulses on lead **58** to the Bit-Clock; no further counting in the timing chain takes place. A short, indeterminate time after the Home flip-flop is set, a SYNC pulse will be read from the memory **38** and transmitted, via a lead **80**, to the reset input of Home flip-flop **60**, thereby placing the flip-flop back in its reset state. The timing chain then proceeds through another cycle of counting until once again at COB2-time the Home flip-flop is set.

At the same time that the Home flip-flop is reset, the SYNC pulse is read into an A-counter (FIGS. **8** and **9**) of the arithmetic unit **40**. Now, at B13-time of CORS-time, the SYNC pulse is transferred to the C-counter and thence back into the memory **38**.

Various arithmetic and data or number manipulation operations require that the timing chain pass through one or more complete cycles. There is, therefore, provided a means for counting cycles of the timing chain, which means is shown in FIG. **5** as Entry Phase Counter **82**. The Entry Phase Counter may be any well-known binary or decade counter that will respond to input pulses or signals on a lead **84**. In one preferred embodiment of the calculator **10** (FIG. **1**), the Entry Phase Counter was a three-stage binary counter capable of being preset to a desired number by signals on a channel **86** and capable of being counted up to seven, then returning to zero and beginning the count over again. The Entry Phase Counter's counting input lead **84** is shown connected to the output of an AND-gate **88**. One input to AND-gate **88** is shown as a lead **90** from the function control logic **46** while the other input to AND-gate **88** is a lead **92** from the column-time counter **74**. A 1-level pulse will be transmitted on lead **92** each C16-time; if the other input (lead **90**) to AND-gate **88** is also 1-level a 1-level incrementing pulse will be transmitted via lead **84** to the input of the Entry Phase Counter. Thus, at each C16-time of a timing cycle, the Entry Phase Counter will be incremented by one. Various logic gates are incorporated in the calculator of the present invention to detect various counts or conditions of the Entry Phase Counter. In order to simplify the drawings and descriptions, some of the Entry Phase Counter count detector gates are not shown but are merely indicated by a lead which is marked with an appropriate legend, such as for example, EPC1 (Entry Phase Counter, count 1). It is within the skill of a person skilled in the art to which the present invention pertains to provide such count detection decoding gates.

In addition to those bit-times, register-times, and column-times generated by the appropriate counters shown in FIG. **5**, a special set of timing signals shown in FIG. **6** as T1, T2, T3, T4, and T5 are generated during the B13, **14**, and **15** times of each register-time. Appropriate gates are incorporated in the system to generate these signals. The use of the signals will be set forth as the description proceeds.

IDLING MODE

Reference is made to FIG. **8**. In this FIG., there is shown the essential operating sections of the arithmetic unit **40**. As shown in the FIG., data exits from the memory **38** into control logic section **131**. The data pulses are then read serially into an A-counter **159**. The A-counter may be any well-known electronic device capable of accepting input pulses and storing such pulses therein as will become more clear as the description proceeds. In the normal idling mode of operation after a complete data word (for example, the data read from C1R1BO-10), a complete data word is read into the A-counter and is parallel shifted into a C-counter **155**. The C-counter may be similar to the A-counter and capable of accepting parallel input and capable of shifting its contents out to a write control **132** and thence back into the memory **38**.

Other shifting operations between the A-counter, D-counter, and C-counter take place during various operations of the apparatus as will be described below. Reference is now made to FIG. **9**. Near the top middle portion of the FIG., there is shown an AND-gate **167** having two inputs, one input of which is from an inverter **169**, the other input of which is the T1-timing signal. Data is read from the memory **38** during each register-time (BO-B1O). The output of inverter **169** is normally 1-level; thus, at each T1-time of each register-time, AND-gate **167** is fully enabled and transmits a 1-level A-to-C signal to the C-counter **155** which causes the contents of the A-counter to be parallel shifted via signal channel **168** to the C-counter. Now, during the next BO-B1O of the next register-time, the contents of the C-counter will be written back into the memory by means of AND-gate **158**. It should be noted, however, that the data shifted serially from the C-counter to the memory would, at first impression, appear to have been delayed by one register-time. However, recalling the SYNC pulse is also read from memory, it is also caused to pass through the A-counter, thence to the C-counter, and back onto the memory and it also is affected by this "1-register-time delay." However, since all data is designated as occupying a bit-space-time compartment in the memory **38**, with reference to the SYNC pulse, the data is automatically correctly aligned

in the memory with respect to the SYNC pulse. Thus, while it is true that there is a 1-register-time delay, the orientation of the data with respect to the SYNC pulse remains the same.

ENTRY OF A WHOLE NUMBER PORTION, FIRST DIGIT

Reference is now made to the simplified logic diagram of FIG. 8. It may be assumed that the operation prior to entry of the first digit of a number was a functional operation, initiated by operation of a function key on the keyboard unit 44. Operation of any function key causes a printout, and a 1-level signal is transmitted from the print control unit 30 (see also FIG. 3) via lead 130 to the set input of a memory means or Common Function Storage flip-flop 134, thereby setting that flip-flop. When the Common Function STORAGE flip-flop 134 is set, a 1-level CFS signal is transmitted on lead 136 to one input of an AND-gate 138. Another input to AND-gate 138 is by way of a lead 140 which is 1-level when the timing control's register counter 70 (FIG. 5) indicates with R1, R2, R3, or R4-time and is 0-level when the register counter indicates an RS or RO-time. Additionally, another input to AND-gate 138 is a lead 116 which will have a 1-level CD signal thereon as soon as any digit key or decimal point key is operated as will be described below. The last input to AND-gate 138 is by way of lead 121 which will have a 1-level EPC3 signal thereon when the Entry Phase Counter (FIG. 5) contains a count of "3."

Depression or actuation of any one of the digit keys on the keyboard (FIG. 1) associated with numerals zero through nine (or decimal point key 14) will immediately cause a set of code signals to be transmitted, in parallel, via a signal channel 100, to a five-stage keyboard buffer-register or set of flip-flops 102. Certain of the stages or flip-flops comprising buffer-register 102 will be set, and certain stages will remain reset, according to a predetermined code implemented by an encoding scheme which is part of the digit key's structure and internal wiring. The five-bit code now contained in the buffer-register 102 will be transmitted to an encoding logic unit 104 which, in turn, will transmit and hold in parallel a five-bit set of code signals, via signal channel 106, to a D-counter 108; no significant action takes place in the D-counter at this time.

At the same time that the buffer-register 102 receives information signals from the keys, a 1-level signal is sent from the operated digit key, via lead 112, to the set input of Common Digit flip-flop 114, thereby setting that flip-flop. Setting of Common Digit flip-flop 114 causes a 1-level CD signal to be transmitted via lead 116 to an input of AND-gates 138, 139, and 141.

The above action takes place at any time during a basic timing cycle. Now when the Entry Phase Counter 82 (FIG. 5) reaches a count of three (COR1BO-time), a 1-level EPC-3 signal is transmitted via lead 121 to AND-gate 138. Also, a 1-level R1 signal is transmitted to the AND-gate 138 via lead 140. The AND-gate 138 is thus completely enabled at this time and transmits a 1-level shift-up (SU) signal via lead 142 to one input of OR-gates 144, 146, 148, and 150.

The OR-gate 148 transmits a 1-level signal to one input of AND-gate 148; OR-gate 144 transmits a 1-level signal to one input of AND-gate 154; and OR-gate 146 transmits a 1-level signal to AND-gate 156.

Now, at the next T1-time which occurs during COR1B13-time, a 1-level D-to-C signal is transmitted from AND-gate 152 to the C-counter 155 via lead 151, thereby causing the contents of the D-counter 108 to be shifted to the C-counter in parallel via a signal channel 153. THe data shifted to the C-counter at this time is not important.

During the COR1 period of time, as above discussed, the B2-B10 data is read from the memory 38 into the A-counter 159. Also, during the above-discussed COR1B2–B10 time, the contents of the C-counter are read into the memory by virtue of a 1-level B0–B12 signal, pulse 1-level clock pulses to AND-gate 158 which, in turn, transmits a train of 1-level signals to the C-counter on a lead 161 which cause the contents of the C-counter to be serially entered into the memory on a lead 160.

Now, at T2-time of the COR1-time under discussion, the AND-gate 154 is fully enabled, thereby transmitting a 1-level clear D-counter (CDC) pulse via lead 162 to the D-counter 108, which pulse causes the D-counter to be cleared or reset to a 0 or no-data condition.

Now, at T3-time of the COR1-time under discussion, AND-gate 156 transmits a 1-level A-to-D-pulse, via lead 157, to the D-counter 108, which pulse causes the contents of the A-counter 159 to be transferred, in parallel, via signal channel 149, to the D-counter. It will be recalled that the A-counter contained COR1B2–B10 data, which data is thus transferred to the D-counter.

From the above, it may be understood that during COR1-time, the first "digit" of Register 1 is read from the memory 38 into the A-counter, a "digit" is read into the memory 38 during the same R1-time (which R1-time becomes RO-time due to the shifting of the SYNC pulse as described previously) from the C-counter, a "digit" is shifted from the D-counter to the C-counter, the D-counter is cleared of data, and the first digit of Register 1 (now in the A-counter) is shifted from the A-counter to the D-counter.

Now, at the next set of B2-B10 times, which occurs during R2-time of the same CO-time discussed above, the first "digit" of Register 2 is read from the memory 38 into the A-counter 159, and a "digit" in the C-counter is read into the COR2-time of the memory (which R2-time becomes R1-time due to the shifting of the SYNC pulse as described previously). Then, at T1-time of COR2-time, the contents of the D-counter 108, which it will be recalled is the first digit of Register 2, is transferred to the C-counter 155. Then, at T2-time, the D-counter is cleared as before. Now, at T3-time, the contents of the A-counter 159, which it will be recalled is the first digit of Register 2, is transferred to the D-counter 108.

At the next set of B2–B10-times, which occurs during R3-time of the CO-time under discussion, the first digit of Register 3 is read from memory into the A-counter 159, and the digit in the C-counter 155, which as described in the immediately preceding paragraph is the first digit of Register 1, is read into the COR3-time of the memory (recall that such R3-time becomes R2-time due to the shifting of the SYNC pulse). Then, at T1-time of COR3-time, the contents of the D-counter 108, which it will be recalled is the first digit of Register 2, is transferred to the C-counter 155. The D-counter 108 is then cleared of data at T2-time. Now, at T3-time, the contents of the A-counter 159, which it will be recalled is the first "digit" of Register 3, is transferred to the D-counter 108.

At the next, or fourth, set of B2-B10, which occurs during R4-time of the CO-time under discussion, the first "digit" of Register 4 is read from memory 38 into the A-counter 159, and the "digit" in the C-counter 155, which as described above is the first digit of Register 2, is read into COR4-time of the memory (recall that R4-time becomes R3-time due to the shifting of the SNYC pulse). Then, at T1-time of COR4-time, the contents of the D-counter, which it will be recalled is the first digit of Register 3, is transferred to the C-counter. At T2-time, the D-counter is cleared of data. At T3-time, the contents of the A-counter, which it will be recalled is the first digit of Register 4, is transferred to the D-counter.

The register-time counter will then advance to RS-time. Thus, the signal on lead 140 will change to 0-level since neither R1, R2, R3, or R4-time is detected from the register-time counter (FIG. 5); AND-gate 138 is thus disabled, thereby transmitting a 0-level signal on lead 142 to the OR-gates 144, 146, 148, and 150. The AND-gates 152, 154 and 156 are thus disabled. However, it is to be especially noted that during the B2-B10-time of RS-time, the contents of the C-counter 155, which it will be recalled from the previous paragraph is the first "digit" of Register 4, is shifted from the C-counter into the C1RS-time of the memory; however, due to the shifting of the SYNC pulse, as described previously, the first digit of Register 3 will thus be occupying COR4-time.

From the above description, it will be understood that data in COR1 is shifted to COR2, the data in COR2 is shifted to COR3, the data in COR3 is shifted to COR4, and the data in COR4 is lost. The same action takes place over and over to cause succeeding digits (C1, C2, C3, etc.) of the first three registers to be transferred or shifted upward into corresponding digit positions of the next higher register, and the content of Register 4 is lost or destroyed in the process.

Now, at the end of C25-time, the column-time counter 74 (FIG. 5) is returned to its zero count (CO); as the column-time counter returns to its zero count, the Entry Phase Counter (FIG. 5) is caused to advance to a count of four. Thus, the EPC–3 signal on lead 121 (FIG. 8) is changed to 0-level, thereby preventing any D-to-C and A-to-D shifting operations since AND-gates 144, 146, 148, and 150 are disabled. However, the data now in the memory is merely circulated in the idle mode of operation, as described previously.

Now, when the Entry Phase Counter is advanced to a count of six (COR3BO-time), a 1-level EPC–6 signal is transmitted to the second input of AND-gate 139; it will be recalled that the other input to AND-gate 139 is 1-level via lead 116 by virtue of the Common Digit flip-flop 114 being in the set state. AND-gate 139 transmits a 1-level K-to-D signal to the D-register via lead 143 which causes the contents of the keyboard flip-flops 102 and encoding logic 104 to be transferred, in parallel, via signal channel 106 to the D-counter. Thus, the code representing the first (most significant) digit of the number to be entered is now in the D-counter.

Now, the Entry Phase Counter 82 (FIG. 5) advances to a count of seven at the next COR3BO-time. When the Entry Phase Counter contains a count of seven, a 1-level EPC–7 signal is transmitted to AND-gate 141. Since the other input to AND-gate 141 is 1-level from the Common Digit flip-flop 114 via lead 116, the AND-gate 141 transmits a 1-level signal on lead 165 to AND-gate 137, AND-gate 147, and the reset input of Common Function flip-flop 134. The other inputs to AND-gate 137 are a lead 145 which will contain a 1-level signal if the decimal point key was not the key pressed; since this section of the description is concerned with entry of a first numerical digit, the lead 145 does have a 1-level signal thereon at this time. Another input to AND-gate 137 is lead 163 which will be 1-level ($\overline{CO\text{-}C2}$) at all times except during C0, C1, and C2-times. The fourth and last input to AND-gate 137 is a lead 164 which is at 1-level during R1-times (from the register-counter 70, FIG. 5). From the above description of the inputs to AND-gate 137, it can be understood that AND-gate 137 will transmit a 1-level signal on its output lead 166 during all EPC–7 R1-times except those R1-times associated with C0, C1, and C2, if the decimal point key was not actuated.

Thus, during C3R1-time, a 1-level signal is transmitted via lead 166 to OR-gates 144, 146, 148, and 150. The OR-gate 148 thus transmits a 1-level signal to AND-gate 152.

During this C3R1-time, the digit data in the associated B2–B10-time is read into the A-counter (this data is zero or aught since a first digit of a number is being entered as described).

Now, at T1-time of C3R1-time, the AND-gate 152 transmits a 1-level D-to-C pulse on output lead 151 which causes the contents of the D-counter (keyboard digit information or data) to be transferred to the C-counter.

Since OR-gate 150 is furnished with a 1-level input signal, its output to inverter 169 is 1-level; this causes inverter 169 to transmit a 0-level signal to AND-gate 167, thereby disabling that AND-gate and thus prohibiting generation of the normal or idling A-to-C 1-level signal on lead 170 at T1-time.

At T2-time of C3R1-time, AND-gate 154 transmits a 1-level CDC pulse to thereby clear the D-counter 108.

Now, at T3-time of C3R1-time, the AND-gate 156 transmits a 1-level A-to-D pulse to the D-counter, thereby causing the contents of the A-counter (C3R1B2–B10) to be parallel shifted into the D-counter. The A-counter is then cleared at T4-time by means of a 1-level signal (Clr A) on lead 172 from AND-gate 171.

Now, during the above-mentioned C3R2B2–B10-times, the contents of the C-counter which, it will be recalled, is the encoded keyboard flip-flop data, are serially shifted into the memory 38 (due to shifting of the SYNC pulse, this data will occupy C3R1B2–B10-times).

Also, during such C3R2-time, the C3R2B2–B10 data is read into the A-counter. Since AND-gate 137 is now disabled by virtue of the fact that the signal on R1 lead 164 is 0-level, AND-gate 167 is enabled by a 1-level signal from inverter 169. Now, at T1-time of C3R2, the contents of the A-counter are parallel shifted to the C-counter. It is to be noted that during R2-times, AND-gate 152 is also disabled by lack of any 1-level signals to OR-gate 148; thus no D-to-C signals are transmitted on lead 151. Additionally, AND-gate 156 is disabled by virtue of the fact that no 1-level signals are present at the inputs of OR-gate 146; thus no A-to-D signal is transmitted on lead 157.

At T2-time, it is to be noted that the D-counter is not cleared of data since no 1-level signals are present on OR-gate 144; thus during R2-time (and also R3, R4, RS, and RO-times immediately following), the C3R1B2–B10 data remains in the D-counter. At T3-time, no significant action takes place. At T4-time, the A-counter is cleared.

Now, during C3R3B2–B10-times, the C3R3 data is serially read into the A-counter, while at the same time, the contents of the C-counter (C3R2 data) is serially shifted into the memory). At T1-time of C3R3, the contents of the A-counter (C3R3 data) is parallel shifted into the C-counter. At T4-time of C3R3, the A-register is cleared.

At C3R4-time, the C3R4B2–B10 data is serially read into the A-register while, at the same time, the contents of the C-counter (C3R3 data) are serially read into the memory.

The same idling action takes place to cause C4RS and C4RO data to be placed back in the memory.

Now, at C4R1-time, AND-gate 137 is once more enabled by the return of a 1-level R1 signal on lead 164. AND-gate 167 is thus disabled while AND-gates 152, 154, and 156 are enabled.

During the B2–B10-times of C4R1, the C4R1 data is read into the A-counter. At T1-time of C4R1, the contents of the D-counter (at this time an aught) is transferred to the C-counter by action of gate 152. At T2-time of C4R1, the D-counter is cleared by action of AND-gate 154. At T3-time of C4R1, the contents of the A-counter are parallel shifted into the D-counter by action of AND-gate 156. At T4-time, the A-counter is cleared by action of AND-gate 171.

Now, during C4R2, C4R3, C4R4-times normal idling transfer action takes place in the same manner as described above.

From the above description, it can be understood that the R1 data for each column-time is shifted left one column-time after entry of a new digit into the C3R1-time, i.e., the Register 1 data read from the memory is delayed one column-time before being written back into the memory.

At the time (EPC–7) that AND-gate 141 transmits a 1-level signal to AND-gates 137 and 147, as just described, a 1-level signal is also sent to the reset input of the Common Function Storage flip-flop 134, thereby resetting that flip-flop. Resetting of flip-flop 134 inhibits any further shift up of register data as controlled by AND-gate 138 described above for the remainder of the digits entered for the first number.

The Entry Phase Counter (FIG. 5) then advances from a count of seven to a count of zero and causes a 1-level EPC-O pulse to be transmitted to the reset input of the common digit flip-flop 114, thereby resetting that flip-flop.

An AND-gate 173 detects the fact that both the common digit flip-flop 117 and common function storage flip-flop 134 are in their reset states and thus a 1-level signal is transmitted from AND-gate 173 via a lead 174 to clear or reset the keyboard flip-flops 102.

Normal idling action of circulating data through the data loop then takes place until further keys are actuated as will now be described.

DECIMAL POINT KEY, FIRST KEY ACTUATED

The decimal point key **14** (FIG. 1) may be the first key actuated (the number to be entered has no whole portion digits), or may be the key actuated after the whole portion digits of a number have been entered. There will now be described the structure and action involved when the decimal point key is the first key actuated.

Operation of the decimal point key **14** causes a 1-level signal to be transmitted on lead **112** to the set input of common digit flip-flop **114**. In addition, a set of signals are transmitted from the keyboard **44** via signal channel **100** to the keyboard flip-flops **102**; at least one of the keyboard flip-flops will be set which identifies and stores the fact that the decimal point key **14** has been actuated. A 1-level decimal point (DP) signal is decoded in the encoding logic unit **104** and transmitted via lead **177** to an AND-gate **175**.

No pertinent action takes place at EPC–0-time nor EPC–1-time.

Now, at EPC–2-time, AND-gate **175** is fully enabled and transmits a 1-level decimal point key (DPK) signal via lead **178** to an inverter **179**, plus the set input of the decimal point storage flip-flop **176**; the flip-flop is thus placed in its set state. It will be noted that the decimal point storage flip-flop **176** is placed previously in its reset state by 1-level signal on lead **130** from the print control unit **30** at the end of the previous printout operation. The 1-level DPS signal to inverter **179** has no significant effect at this time.

At EPC–3-time, AND-gate **138** is enabled since the common digit flip-flop **114** is in the reset state. Thus, action exactly like that described above for entry of a first numeral digit of a whole portion of a number will take place to shift the contents of Register **1** to Register **2**, shift the contents of Register **2** to Register **3**, and shift the contents of Register **3** to Register **4**.

No significant action takes place at EPC–4-time nor EPC–5-time. At EPC-6-time, the contents of the keyboard flip-flops are entered into the D-counter since AND-gate **139** is enabled; however, the contents of the D-counter will be subsequently cleared and thus, no data corresponding to the set state of the keyboard flip-flops is entered into the memory **38**.

At EPC–7-time, the Common Function Storage flip-flop **134** is reset by a 1-level signal from AND-gate **141**.

Also at EPC–7-time, the AND-gate **175** is enabled, thereby transmitting a 1-level DPK signal to inverter **179** which, in turn, transmits a 0-level disabling signal on lead **145** to AND-gate **137**. Since AND-gate **137** is now disabled, no shifting of the contents of Register **1** one column-time to the right will take place. It is to be noted that AND-gate **147** is also disabled by the 0-level signal on lead **145** at this EPC–7-time.

The entry phase counter (FIG. **5**) then is advanced to a count of zero. The common digit flip-flop **114** is reset by the 1-level EPC–0-signal. Since both the common digit flip-flop **114** and the Common Function Storage flip-flop **134** are now in the reset state, AND-gate **173** is enabled fully and transmits a 1-level signal on lead **174** to reset the keyboard flip-flops **102**.

DECIMAL POINT KEY ACTUATION SUBSEQUENT TO DIGIT KEY OPERATION

If the decimal point key **14** is operated subsequent to a digit key operation (the number being entered has a whole number portion), the following action differing from that described above takes place.

It will be recalled that when a digit key is actuated, the Common Function Storage flip-flop **134** is reset and will not be set again until the end of another printout operation. Thus, at EPC-3-time, after the decimal point key has been actuated, AND-gate **138** is disabled and the Registers **1**, **2**, **3**, and **4** will not be shifted upward. Except for this difference, the action as described previously takes place.

DIGIT KEY ACTUATION, DECIMAL FRACTION PORTION

If the Decimal Point Storage flip-flop **176** has been set by operation of the decimal point key **14** as described above, and then a digit key is operated, the following described action takes place.

Action at ECO-**1**, -**2**, -**3**, -**4**, -**5**, and -**6** times takes place in the same manner as described previously for operation of digit key (whole number portion, first digit or subsequent digits).

Now, at EPC-7-time, AND-gate **141** is enabled, thereby transmitting a 1-level signal via lead **165** to AND-gate **147**, AND-gate **137**, and the reset input of Common Function Storage flip-flop **134**. The Common Storage flip-flop is already in the reset state having been placed in such reset state by the previous operation of either a digit key or the decimal point key.

AND-gate **175** is disabled since the signal on lead **177** is 0-level from the encoding logic **104** (a key other than the decimal point key is being actuated). Thus, a 0-level signal is transmitted from the AND-gate **175** to inverter **179** which, in turn, transmits a 1-level signal on lead **145** to AND-gate **137**, plus AND-gate **147**.

The decimal point storage flip-flop is in the set state having been placed in such set state by the previous operation of the decimal point key and thus transmits a 1-level signal on set output lead **180** to AND-gate **147**.

Thus, at C2RO-time, AND-gate **147** is enabled completely and transmits a 1-level signal on lead **181** to AND-gate **182** and inverter **183**. Inverter **183** thus transmits a 0-level disabling signal on lead **184** to AND-gate **171**; there will thus be no 1-level clear A-counter (Clr A) transmitted to the A-counter during this C2ROT4-time.

Now, during T4-time of C2R0-time, AND-gate **182** transmits a 1-level preset A-counter to one signal (A-to-1) to the A-counter. This 1-level A-to-1 signal clears the A-counter of any data that may be contained therein and presets it to a count of one. The count of one is indicative of the fact that a digit key has been operated after the decimal point key has been operated.

Now, the timing chain is advanced to C2R1-time. AND-gate **147** is thus disabled.

During the C2R1B0–B10 the contents of C2R1 are read into the A-counter **159**. THe contents of C2R1 are a count or record of how many prior digit keys have been operated subsequent to operation of the decimal point key. Thus, if the digit key currently being operated is the first digit key operated subsequent to operation of the decimal point key, the contents of C2R1B0–B10 now being entered into the A-counter will be zero. On the other hand, if the digit key currently operated is, for example, the fourth digit key operated subsequent to operation of the decimal point key, the contents of C2R1 being entered into the A-counter at this time are a "three."

The C2R1 data or count entered into the A-counter is added to the contents of the A-counter. It will be recalled that the A-counter has been preset with a count of "one." Therefore, the contents of C2R1 are added to a "one." Or, to express it another way, the contents of C2R1 are incremented by "one."

AND-gate **137** is disabled at C2-time. AND-gate **138** is disabled during this EPC–7-time. Therefore, OR-gate **150** has no 1-level inputs and thus transmits a 0-level output to inverter **169** which, in turn, transmits a 1-level signal to AND-gate **167**. At T1-time of C2R1, a 1-level A-to-C signal is transmitted via lead **170** to the C-counter, thereby causing the contents of the A-counter to be parallel shifted to the C-counter. It will be recalled that at this time, the contents of the A-counter are the former contents of C2R1 incremented by one. The register counter then advances to a count of R2 and in doing so, the contents of C2R2B0–B10 are read into the A-counter, etc., thus, the normal idling mode of operation as previously

described. The register counter finally is advanced to a count of two indicative of RS-time. When the register counter changes to a count to two, the column-time counter is changed to a count of three indicative of column-3-time. Idling mode action continues until the register time counter now reaches a count of four indicative of R1-time. AND-gate **137** is now fully enabled and, thus, AND-gate **152** rather than AND-gate **167** is enabled; thus, AND-gate **152** transmits a 1-level D-to-C signal on lead **151** to the C-counter at C3R1-time. During this same C3R1-time, the C3R1 contents of the delay line are being read into the A-counter. It may be recalled that the contents of the D-counter at this time are the coded signal received from the keyboard flip-flops during the previous EPC–6-time. Thus, it will be recognized that that action which has been described above for entering the contents of the keyboard flip-flops into C3R1-time takes place and the contents of Register 1 are shifted one place or column-time to the left as described previously.

PRINTOUT OF AN ENTERED NUMBER

After a number has been entered into Register 1, as described above, a function key, such as for example, the Add key **17** (FIG. 1) is actuated, or the first number entry key **16** (FIG. 1) is actuated. Actuation of either a function key or the first number entry key will cause printout of the number thus contained in Register 1. The printout will be exactly as the number was entered; i.e., if there were six digit keys actuated subsequent to actuation of the decimal point key, the number will be printed out with six digits to the right of decimal point.

According to another feature of the present invention, the printout will be such that the digits printed to the left of the decimal point will be in sets of three digits, each set being spaced from adjacent sets by a space as shown in FIG. 2.

Reference is now made to FIG. 10. FIG. 10 includes a simplified schematic of the mechanical structure in one form of printer utilized with the present invention. Only those mechanical details necessary to an understanding of the present invention are shown and described herein. Further details of the printer utilized in the preferred embodiment of the present invention are shown and described in copending U.S. Pat. application Ser. No. 663,292, filed Aug. 25, 1967 by L. D. Chamness and A. F. Marion now U.S. Pat. No. 3,406,625 issued Oct. 22, 1968 which is a continuation-in-part of U.S. Pat. application Ser. No. 528,501, filed Feb. 18, 1966 by L. D. Chamness and A. F. Marion for "High Speed Printing Apparatus" now abandoned; both of said applications being assigned to the same assignee as the present application. Another copending U.S. patent application showing various other mechanical details of a printer of the type utilized in the preferred embodiment of the present invention is U.S. Pat. application Ser. No. 650,501, filed June 30, 1967 by L. D. Chamness, A. F. Marion and K. H. Steward for "Inking Device" now U.S. Pat. No. 3,526,309 issued Sept. 1, 1970; another application showing still other details of a printer utilized with the present invention is U.S. Pat. application Ser. No. 724,880, filed Apr. 29,1968 by L. D. Chamness for "-Printing Means" now abandoned. Both of the latter mentioned copending applications are also assigned to the same assignee as the present application.

Briefly described, the printing apparatus **30** includes an electric motor **191** to which a font wheel mounting and rotating shaft **192** are operatively coupled for rotation when the motor is energized as will be described below.

A carriage drive member **193** is suitably mounted for synchronized rotation with the shaft **192** by suitable means, such as for example, tooth pulley and belt combination **194**. The member **193** is formed with a helical groove **194** having a predetermined pitch and sense.

It will be noted that the shaft **192** and member **193** are mounted for rotation about parallel spaced-apart axes.

A carriage **195** is mounted by suitable means (not shown) for reciprocating movement in a path of travel parallel with the axes of rotation of shaft **192** and screw member **193**.

A solenoid-actuated drive pin **196** is mounted on the carriage **195** for selective movement into and out of the helical groove **194**. It will be understood that with the screw member rotating counterclockwise about its axis as shown by arrow **197** when the drive pin **196** is inserted into the groove **194**, the carriage **195** will be driven from right-to-left which is the normal printing direction. A biasing spring (not shown) normally biases the carriage in the rightward direction. Thus, if the drive pin is pulled out of engagement **196** with the groove **194** while the carriage is being moved to the left, the carriage will be returned to its right-hand or home position.

The longitudinal extent of the shaft **192** is square shaped in cross section. A disclike font wheel **199** is mounted on the square-shaped portion of the shaft **192** such that the font wheel rotates with the shaft and is movable axially along the shaft.

A yokelike member **198** is mounted on the carriage **195** and extends upward alongside the font wheel where it engages with a hub on the wheel. Thus, as the carriage **195** is moved back and forth, as described above, the yoke members act on the font wheel **197** and cause a like amount of right or left movement of the font wheel.

The radially outer periphery of the font wheel is formed or has suitably attached thereto a plurality of character types equally spaced circumferentially thereabout and axially offset from each other such that the geometrical arrangement is like that of a helix. The sense of the helix is opposite to the sense of the helical groove **194** of carriage drive member **193** for reasons that will be made clear in the discussion below. In the preferred printer used in one embodiment of the present invention there are two partial turn helix patterns of characters on the font wheel which provide for different character-to-character spacing between the printout for some of characters.

The pitch of the helical arrangement of the printing types provides for constant rotation of the wheel **199** and axial movement of the carriage **195** across the printing line and yet provide predetermined character-to-character spacing.

A print hammer **200** is energized at appropriate times by a solenoid **201** to cause the paper **31** to be driven into printing contact with the correct type on the print wheel.

Actuation of any of the function keys **44** causes the motor **191** to be energized by means of a motor start circuit **203**. Rotation of the shaft **192** causes rotation of a timing wheel **205** and as a Digit Home tooth or dog **207** passes by a sensor **209**, a Home signal is generated on a lead and transmitted to a Decimal Point Counter (DPC) **211**, thereby causing a count of one to be entered.

A count detector **214** detects a count of one in the DPC counter **211** and transmits a signal to a carriage start circuit **213** which causes the pin **196** to engage with the now rotating screw or helical groove **194**. The carriage is thus moved to the left in synchronism with the rotation of the font wheel **199**.

In addition, the content of the first register R1 is copied into the next lower register RO and the thus new content of register RO is shifted one column-time (C-time) to the left (except C3) according to the shifting principles described previously.

The next four revolutions of the timing wheel **205** advance the DPC counter to a count of five. No significant action takes place during these times insofar as printing of numerals are concerned. However, symbols are printed during these times.

When the DPC count detector **214** detects a count of five, a gating means shown as AND-gate **216** causes the count of nine to be added to the contents of C3RO which, it will be recalled, contains the count representing the number of decimal places in the entered number. Such addition will not cause a carry if the sum is greater than nine.

The contents of C3RO are then shifted to the C-counter **155** (FIG. 8). During this time, the A-counter (C3RO) is sampled to determine if it contains a count of nine; if it does, a decimal point flip-flop **215** is set to thereby cause printing of a decimal point. If the A-counter does not contain a count of nine, further action to print a numeral takes place as now described.

The contents of the A-counter **159** are then shifted to the D-counter **108**. A compare gate **217** compares the count in the decimal point counter with the C-times and renders and provides for gating of character pulses from a character transducer **219** adjacent the timing wheel **205** into the D-counter for counting down the contents of the D-counter.

The first digit to be printed is in C5RO-time and the DPC is at a count of five at this time. Thus, the contents of the D-counter when C5RO is contained therein will be counted down to zero. A detector gate **220** detects when the contents of the D-counter are zero and transmits a hammer driver signal to the print hammer solenoid **201**, thereby causing printing contact between the paper and the now correctly positioned printing type on the font wheel **199**.

At the next occurrence or movement of the Digit Home dog **207** past its associated transducer **209**, the decimal point counter **211** is advanced by one count and the above-described action takes place again to cause the next digit to be printed.

From the above description, it can be understood that adding of nine to the C3RO contents of the A-counter actually counts the contents of C3R0 down by one. Now, when the content of the A-counter is nine, after the addition of nine thereto, this is an indication that the decimal point is to be printed as will now be described.

When the A-counter **159** contains a count of nine, the decimal point flip-flop **215** is set. Setting of the decimal point flip-flop transmits an inhibit (INH) signal to the decimal point counter **211** to prevent advancing of the counter at the next revolution of the timing wheel and also prevents shifting of information from the A-counter to the D-counter at this time.

Setting of the decimal point flip-flop **215** causes setting of a Print Decimal Point (PDP) flip-flop **222** at the next Digit Home signal generated at the next revolution of the timing wheel.

Setting of the Print Decimal Point flip-flop **222** causes the D-counter to be cleared to zero; this action causes the print hammer to be energized at this time, the type in position to be printed is a decimal point. A decimal point is printed.

Shortly thereafter (less than 1 revolution of the timing wheel), a Symbol Home signal is generated from transducer **225** adjacent the timing wheel **205** and causes resetting of the Decimal Point flip-flop **215**.

The Symbol Home signal also enters a count of one into a Space Counter (SCT) **226** which is enabled by the set condition of the Print Decimal Point counter **222**. The space counter will control printing of numeral symbols to the left of the decimal point in groups of three.

Resetting of the Decimal Point flip-flop **215** enables the decimal point counter **211** to be advanced at the next Digit Home signal and enables the D-counter to accept new data.

Appropriate digit data from RO as determined from the decimal point counter **211** and gate **217** is now entered into the D-counter **108**.

Printing action like that described previously now causes a numeral which is the least significant digit of the whole number portion of the number in register RO (copied from register **R1**) to be printed.

The Digit Home signal will then cause the decimal point counter **211** to be advanced as described previously.

However, it is to be noted that since the Print Decimal Point flip-flop **222** is now in the set state, a signal is sent from that flip-flop to disable AND-gate **216**; thus, a count of nine will not be added to the A-counter for the remainder of the printing function.

Now, at the next Symbol Home signal, the space counter **226** will be advanced to a count of two.

The next (second) digit of the whole number portion to be printed is entered into the D-counter as described before and will be printed.

At the next Digit Home signal, the decimal point counter **211** will be advanced by one and this action causes the next (second) digit of the whole number portion to be printed.

Now, at the next Symbol Home signal, the space counter **226** is advanced to a count of three.

Now, at the next Digit Home signal, the next (third) digit of the whole number portion is printed as described previously. The Symbol Home signal generated immediately after the third digit is printed causes the space counter **226** to be counted to zero or cleared.

When the space counter **226** is advanced from a count of three to a count of zero, an inhibit or "0" signal is transmitted to the Decimal Point Counter **211**, thereby preventing that counter from being advanced at the next Digit Home signal. This space or "0" signal also disables AND-gate **217**. Thus, the contents of the D-counter are not counted down and thus no digit will be printed.

The type wheel **199** continues to advance to the left and the timing wheel **205** continues to rotate. Thus, the type wheel advances leftwardly across the paper by a character-to-character or symbol-to-symbol "space."

Now, at the next Symbol Home signal, the space counter **226** is advanced to a count of one. Thus, the inhibiting "0" signal is removed from the Decimal Point Counter **211** and the AND-gate **217**.

The system is thus enabled to print the contents of the D-counter (the fourth digit of the whole number portion) in the same manner as described previously.

It will be understood that the above-described action takes place over and over to print the whole number portion digits in groups of three.

A most significant digit detector **230** is set when the most significant digit of the number is printed. Such most significant digit is detected by noting the absence of any data in register RO at the appropriate C-times. When such condition is encountered, it is desired to inhibit printing of the symbols for "-zero."

When the most significant digit is detected as having been printed, a signal is transmitted to the carriage start circuit **213** and motor start circuit **203**, thereby causing the motor **191** to turn off and the carriage to be returned to the right under action of a biasing spring (not shown). In addition, the most significant digit detector resets the printing circuits in preparation for another cycle of printing operation.

READ STACK

It is often desirable to cause the entire contents of the registers **R1**, **R2**, **R3**, and **R4** to be printed out as a group and to do so without destroying the contents of these four registers. This ability or feature is desirable when it is desired to check intermediate results or entry of numbers that are in the upper three registers (**R2**, **R3**, and **R4**). The read stack operation is accomplished in the manner now to be described.

Upon the second actuation of the first number entry key without an intervening actuation of an arithmetic function key, or an actuation of the first number entry key immediately after actuation of a key that causes entry of a new number into the first register **R1**, such as for example, a duplicate key or a recall from memory key, will cause enabling of a read stack circuit **235**. This circuit will then cause the contents of the fourth register **R4** to be transferred to the register RO in a like manner as described previously for printing of the contents of register **R1**. In addition, the motor start circuit **203** will be energized by a signal from the read stack circuit, thereby causing the motor to start rotation of the type wheel **199** and timing wheel **205** so as to cause printout of the new contents of register **R0** in a manner like that described previously.

After the contents of **R0** are printed, the read stack circuit causes the contents of register **R3** to be copied into the **R0** register and printed.

After the contents of **R0** are printed (copied from **R3**), the read stack circuit causes the contents of register **R2** to be copied into register **R0** and printed.

After the contents of **R0** (copied from **R1**) are printed, the read stack circuit **235** causes the contents of register **R1** to be

copied into the R0 register and printed. At the end of this printing, the printing operation is ceased in the same manner as described before.

While the principles of the invention have been made clear in the illustrative embodiments, there will be obvious to those skilled in the art, many modifications in structure, arrangement, proportions, the elements, materials, and components used in the practice of the invention, and otherwise, which are adapted for specific envisionments and operating requirements, without departing from these principles. The appended claims are, therefore, intended to cover and embrace any such modifications within the limits only of the true spirit and scope of the invention.

What is claimed is:

1. In an apparatus for handling a number having a maximum quantity of digits, each digit being one of the first 10 cardinal numerals, the combination comprising:
- a first means for storing the digits of a first number;
- second means for storing a second number indicative of the quantity of decimal fraction digits in the number stored in said first storage means;
- means for initiating the printing of the contents of said first storage means;
- means for printing the individual cardinal numeral symbol associated with successive ones of the digits in said first storage means;
- means for incrementing the contents of said second means for each printed cardinal numeral symbol;
- means for comparing said contents with a predetermined number;
- means for generating a decimal point print signal when said contents and said predetermined number are equal;
- said printing means including means responsive to said decimal point print signal for effecting the printing of a decimal point symbol.

2. In an apparatus according to claim 1 wherein:
- said first storage means is a multistage storage means having as many stages as said maximum quantity of digits of said first number, individual digits of said first number occupying individual stages of said first storage means.

3. In an apparatus according to claim 2 wherein said first storage means and said second storage means include an acoustic delay line.

4. In an apparatus according to claim 2 wherein there is further included a single digit storage means coupled to said printing means, and
- means responsive to said printing initiating means for transferring, one by one, in a predetermined order, the digits stored in said first storage means to said single digit storage means;
- said printing means printing the individual cardinal numeral symbol associated with the digit transferred into said single digit storage means.

5. In an apparatus according to claim 1 wherein said predetermined number is nine.

6. In an apparatus according to claim 1 wherein said means for incrementing includes means for adding the numeral nine to said contents.

7. In an apparatus according to claim 1 wherein said first and second storage means are implemented on an information-recirculating delay line.

8. In an apparatus according to claim 1 wherein there is further included a set of manually operable switches for effecting entry of digits, one by one, into said first storage means;
- a manually operable decimal point indicative switch;
- means responsive to the operation of said decimal point indicative switch for counting the number of times individual ones of said set of manually operable switches are operated subsequent to operation of said decimal point indicative switch and for entering said count of the number of times said manually operable switches are operated into said second storage means.

9. In an apparatus for handling a number having a maximum quantity of digits, each digit being one of the first 10 cardinal numerals, the combination comprising:
- a first storage means for storing the digits of a first number;
- means for initiating the printing of the contents of said storage means;
- means for printing the individual cardinal numeral symbol associated with the individual digits of the number stored in said storage means, said printing means including spacing means for selectively printing adjacent symbols with a normal symbol-to-symbol spacing, and control means for altering said spacing in response to a first signal; and
- cyclical counting means coupled to said printing means for counting the quantity of symbols printed after operation of said printing-initiating means and for generating said first signal when a predetermined count is contained therein, wherein the cardinal numeral symbols associated with a number in said storage means are printed in groups, each group being separated from adjacent groups by a greater than normal symbol-to-symbol spacing.

10. In an apparatus according to claim 9 wherein said storage means includes an information recirculating delay line.

11. In an apparatus according to claim 9 wherein said cyclical counting means comprises a scale of three counter.

12. In an apparatus according to claim 9 wherein there is further included:
- second means for storing a second number indicative of the quantity of decimal fraction digits in the number stored in said first storage means;
- means for comparing the number stored in said second storage means with the quantity of times a cardinal numeral symbol is printed after operation of and in response to said means for initiating printing, said means for comparing generating a second signal when the number of times a cardinal numeral symbol is printed by said printing means is equal to the number contained in said second storage means;
- said printing means being responsive to said second signal for effecting the printing of a decimal point symbol; and
- means for rendering said cyclical counting means nonoperative until the occurrence of said second signal.

13. In an apparatus for handling a plurality of numbers, each number having a maximum quantity of digits, the combination comprising:
- a plurality of storage means;
- means for entering a number into a first one of said storage means, said number-entering means including means for transferring the contents of certain ones of said storage means into certain other ones of said storage means as a number is entered into said first one of said storage means;
- means for printing the cardinal numeral symbols associated with the individual digits of the numbers stored in said storage means;
- means for initiating printing of the number stored in said first storage means; and
- means conditioned by the printing of the number stored in said first storage means for initiating printing of each of the numbers stored in each of said storage means according to a predetermined order.

14. In an apparatus according to claim 13 wherein said means for entering a number into said first storage means includes a set of manually operable cardinal numeral representing switches, and wherein said means for initiating printing includes a manually operable switch means.

15. In an apparatus according to claim 13 wherein each of said storage means includes means for storing a value indicative of the quantity of decimal fraction digits in the number stored in the associated storage means;
- means for incrementing the contents of each of said value-storing means for each printed cardinal numeral symbol corresponding to said number in said associated storage means;

means for comparing said contents with a predetermined number;

means for generating a decimal point print signal when said contents and said predetermined number are equal;

said printing means including means responsive to said decimal point print signal for effecting the printing of a decimal point symbol.

16. In an apparatus according to claim 13 wherein said printing means includes spacing means for selectively printing adjacent symbols with a normal symbol-to-symbol spacing, and control means for altering said spacing in response to a first signal;

cyclical counting means coupled to said printing means for counting the quantity of symbols printed as each number stored in each of said storage means is printed and for generating said first signal when a predetermined count is contained therein, wherein the cardinal numeral symbols associated with the numbers in each of said storage means are printed in groups, each group being separated from adjacent groups by a greater than normal symbol-to-symbol spacing; and

means for resetting said cyclical counting means to an initial state after said symbol corresponding to the most significant digit of said each number has been printed.

17. In an apparatus according to claim 16 wherein said cyclical counting means comprises a scale of three counter.

18. In an apparatus according to claim 13 wherein said each of said storage means includes means for storing a value indicative of the quantity of decimal fraction digits in the number stored in the associated storage means;

means for incrementing the contents of each of said value-storing means for each printed cardinal numeral symbol corresponding to said number in said associated storage means;

means for comparing said contents with a predetermined number;

means for generating a decimal point print signal when said contents and said predetermined number are equal;

said printing means including means responsive to said decimal point print signal for effecting the printing of a decimal point symbol;

said printing means including spacing means for selectively printing adjacent symbols associated with a number being printed with a normal symbol-to-symbol spacing, and control means for altering said spacing in response to a second signal;

cyclical counting means coupled to said printing means for counting the quantity of symbols printed subsequent to printing of said decimal point symbol as each number stored in each of said storage means is printed and for generating said second signal when a predetermined count is contained therein, wherein the cardinal numeral symbol associated with the whole number portion of the numbers in each of said storage means are printed in groups, each group being separated from adjacent groups by a greater than normal symbol-to-symbol spacing; and

means for resetting said cyclical counting means to an initial state after said symbol corresponding to the most significant digit of said each number has been printed.

19. In an apparatus according to claim 18 wherein said cyclical counting means comprises a scale of three counter.

20. In an apparatus according to claim 1 wherein said printing-initiating means includes a manually operable switch means, and said printing means includes a type wheel secured to a rotatably mounted shaft;

power means for rotating said shaft; and

means for energizing said power means in response to operation of said manually operable switch means.

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