The bistable multivibrator (or flip-flop, Eccles-Jordan circuit, or binary, as it is variously called) is the backbone of the digital computer and calculator. Its applications are legion, and its design variations are only slightly less numerous, if indeed at all. But, being derived from a basic design, all variations have a great deal in common and, thus, can be studied as a group. The bistable is so called, because it has two stable states, but the term, "flip-flop", is just as common in usage and will be used here.

Consider the circuit in Figure 1. The two halves of the circuit are identical, with corresponding components equal in value. That is, the load resistor of Q1 is equal to the load resistor of Q2. Similarly, R3 = R4 and R5 = R6. Assume for the moment that Q1 is on. The voltage on its collector is 0 volts. It becomes apparent that R3 and R6 comprise a voltage divider from 0 volts to +6 volts. This puts some positive voltage on the base of Q2. Any positive voltage on the base of Q2 keeps it turned off. With Q2 off, another voltage divider is comprised of R2, R4, and R5 from -12 volts to +6 volts. The values of these resistors are such that the base of Q1 is negative, which keeps Q1 on. This state is stable; that is, the flip-flop will remain in this state for an indefinite period of time. With corresponding resistors equal in value, it is self-evident that another stable state can be found by assuming that Q2 is on instead of Q1.

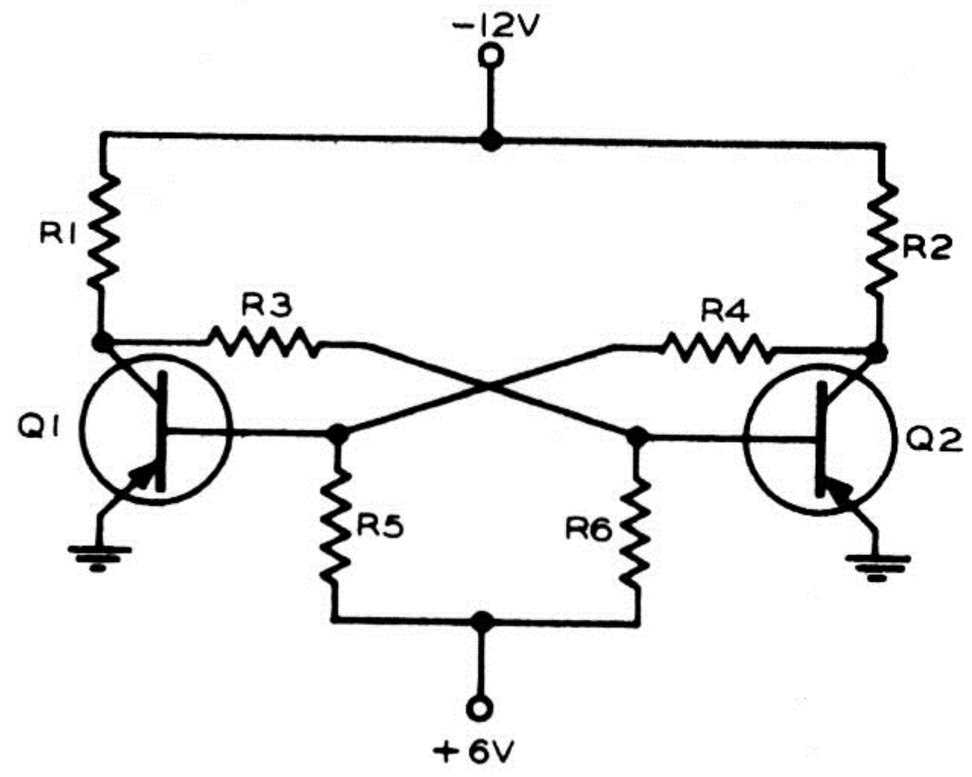


Figure 1 - A BASIC FLIP-FLOP

It might be expected that, since the circuit is symmetrical (corresponding components equal), there is a third stable state where the currents through the transistors are equal creating equal base currents and bias voltages. While it is true that this condition can exist, it is not true that it is a stable state. Suppose that there is a very small decrease in the collector current of Q1. Then the collector voltage of Q1 will increase a very small amount. Q2 will see this as a tiny increase in base current, and will amplify it. This increases the collector current of Q2, and decreases the collector voltage. Q1 sees this as a decrease in base current, and this decrease is amplified by Q1. The collector current of Q1 is further decreased, and this cycle continues until a stable state is reached. In this case, the stable state will be with Q1 off and Q2 on, but it might just as easily have gone the other way. This leads to the conclusion that the flip-flop has ONLY two stable states, and that it will normally be in one of these two states.

Assume that the flip-flop is in the stable state with Q1 on and Q2 off. If Q1 is removed from the circuit by removing it from its socket, then the base of Q2 will go negative and Q2 will turn on. Now the junction of R4 and R5 (where the base of Q1 is normally connected) is positive. If Q1 is now returned to the circuit, Q1 will be off, and Q2 will remain on. A permanent transition will have been effected. This is not, however, considered an efficient means of flipping the flip-flop. Again, consider Q1 on and Q2 off. If the base of Q1 is shorted to +6 volts, it will turn off. This permits the collector of Q1 to go to -12V which forward biases the base of Q2 and turns it on. When Q2 turns on, the +6 volts can be removed from the base of Q1, because Q1 is now biased off by Q2 being on. Again, a transition has been effected.

In the last example, the signal (+6 volts) was maintained on the base of Q1 until Q2 was fully on and some positive voltage was being put on the base of Q1 by the voltage divider R4, R5. This transition takes a finite period of time. If the length of time that +6 volts is applied to the base of Q1 is much shorter than the transition time, then the transition may not be effected at all. If the collector voltage of Q1 just starts to increase, and then the +6 volts is removed from the base, then Q1 may still be conducting harder than Q2 which will be just starting to turn on. In other words, if the flip-flop has a long (relatively) transition time, it won't be able to respond to very short pulses. The solution is to shorten the transition time.

One solution to the problem of long transition times is the "commutating" capacitor. Because of its effect upon the circuit, it is generally called a "speed-up" capacitor. Other names are "cross-

coupling" and "transpose" capacitor. The effect of their presence in the circuit is to couple the 12 volt transition pulse from the collector of one transistor to the base of the other without the attenuation associated with cross-coupling resistors (R3 and R4). However, the cross-coupling resistors are still there to provide D.C. bias as previously described. Figure 2 shows a flip-flop with speed-up capacitors.

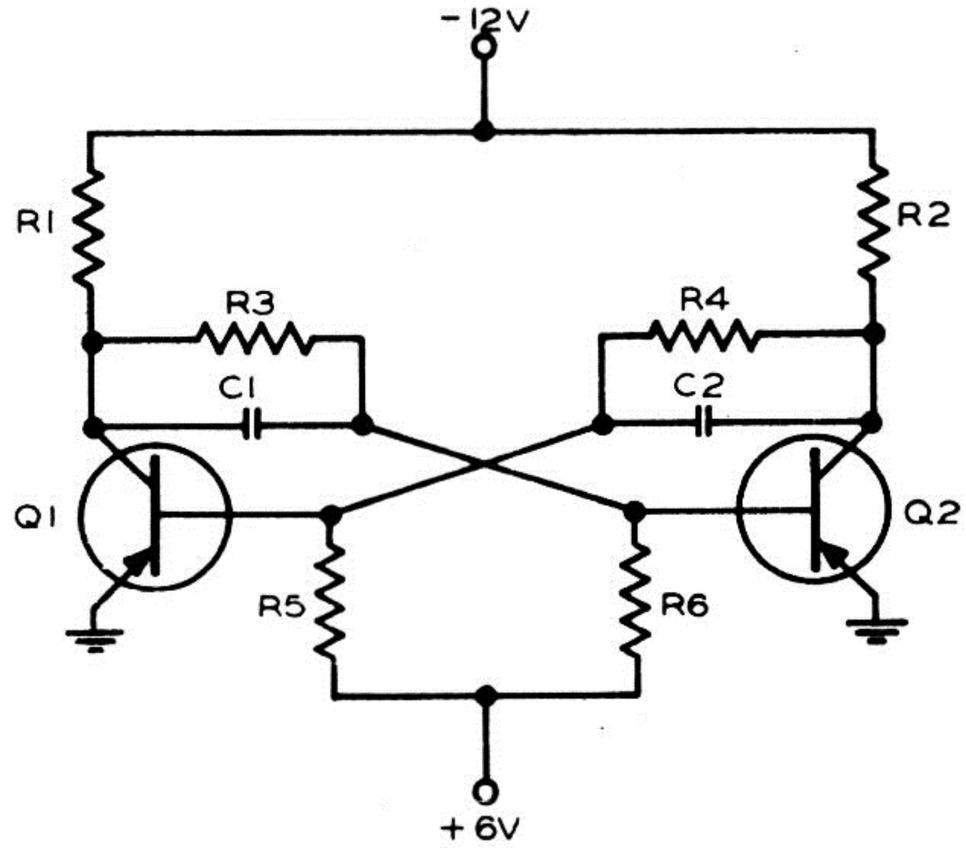


FIGURE 2 - APPLICATION OF COMMUTATING CAPACITORS

The speed-up capacitors drastically decrease the transition time of the flip-flop. With them, the circuit can be flipped with a much shorter pulse than with just the cross-coupling resistors.

Next comes a more detailed analysis of the inputs. There are two basic types of triggers; unsymmetrical, and symmetrical. The unsymmetrical trigger will be considered first. The term, "unsymmetrical", refers, not to the waveform of the trigger pulse, but to the method by which it is introduced to the flip-flop. An unsymmetrical trigger will effect a transition in one direction only.

A second unsymmetrical trigger must be introduced in different parts of the circuit to effect transition in the opposite direction. Figure 3 shows a flip-flop with an unsymmetrical trigger input. The trigger circuit is comprised of a capacitor, a resistor, and a diode connected to the base of Q1. Assuming that Q1 is on, consider the static condition with a -12 volt level input to C3. The base of Q1 is at about -.2 volts. The capacitor C3 is charged to -12 volts with 0 volts on its right side. If the -12 volts level rises to 0 volts very rapidly, the right side of the capacitor must go to 12 volts in order to maintain the relative charge of C3. (See Friden Electronic Course, Lesson 5, for a more complete description of RC circuits). 12 volts forward biases the diode, and 12 volts on the base of Q1 turns it off and the stage flips. There is nothing in the rule books that says that 12 volts will remain on the right side of C3. The 12 volts will, in fact, bleed through R7, and the final charge on C3, assuming that 0 volts remains the input, will be 0 volts on both sides of C3. If the input now returns to -12 volts, then -12 volts will be felt on the anode of the diode which will back bias it. Therefore, the -12 volt pulse will have no effect on the circuit. If it were allowed on the base of Q1, the negative pulse would turn Q1 back on which would negate the very purpose of the flip-flop. Figure 4 shows the time relationship of input to output pulses and the effect of C3, R7, and D1.

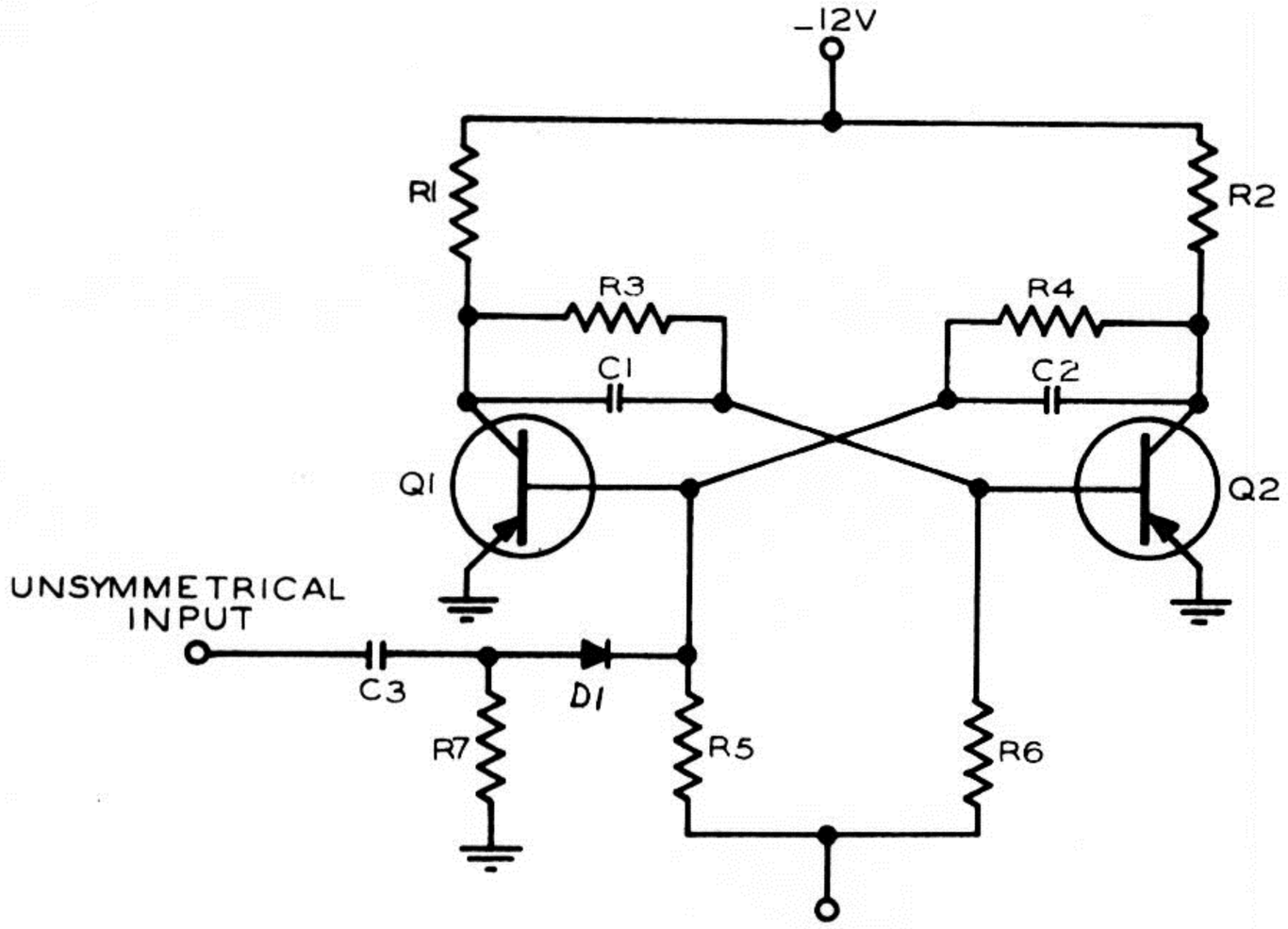


FIGURE 3 - Unsymmetrical Trigger Input

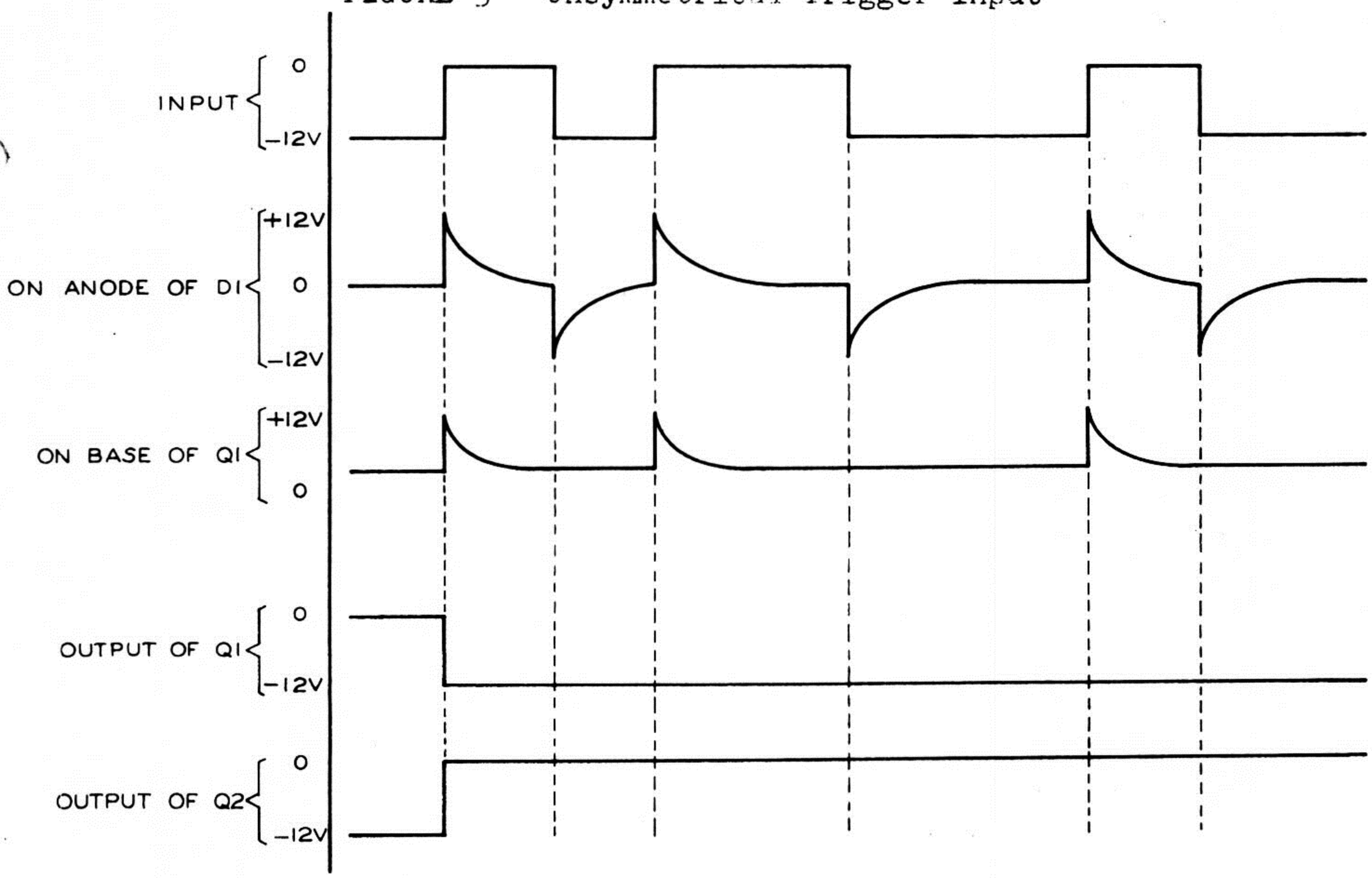


FIGURE 4 - Waveforms of a Flip-Flop With an Unsymmetrical Input

Note that repetitive triggers into the unsymmetrical triggering circuit have no effect on the state of the flip-flop. The first positive pulse on the base of Q1 flipped the stage, the negative-going pulses were blocked by D1, and nothing has flipped the stage back to the original condition of Q1 on, Q2 off. Thus far, R7 has been shown as the discharge path of C3, always returning the right side of C3 to 0 volts. But, it should be clearly understood that R7 is also the CHARGE path. The significance of this becomes apparent if R7 is mentally returned to -12 volts for a moment. With 0 volts input, the right side of C3 is -12 volts. If the input goes to -12 volts, then the right side of C3 must go to -24 volts. The diode is back biased, so there is no effect of the -24 volt pulse on the flip-flop. But the right side of C3 returns to -12 volts through R7. Now, when the input goes to 0 volts, the right side of C3 also goes to 0 volts, not to 12 volts. There is no positive pulse, hence the flip-flop will not flip. Now, it becomes apparent that if R7 is tied to the collector of a transistor, it becomes a permissive gate. When this transistor is on, R7 is grounded and permisses the stage to be flipped by an input trigger to C3. If the transistor is off, R7 is returned to -12 volts, and will not allow C3 to develop a positive pulse. Hence, the trigger is inhibited. This is the way the unsymmetrical input is generally used, and the discovery of an unsymmetrical input with signals applied to both the capacitor and resistor should not cause even the mildest feeling of alarm or panic.

This, then, is unsymmetrical triggering. It follows that another trigger circuit can be connected to Q2 for similar results with resulting transition in the opposite direction. Figure 5a shows an

unsymmetrical triggering circuit connected to each base with both capacitors and resistors shown as signal inputs, and no further explanation will be deemed necessary.

The symmetrical trigger input circuit, often called the "T" input, is remarkably similar to the unsymmetrical input. Comparison of Figures 5a and 5b reveals that the symmetrical input can be made from two unsymmetrical input circuits by connecting each input resistor to the appropriate collector, and connecting the capacitors together. The flip-flop, then, provides the level input necessary to gate the proper capacitor. Consider the circuit in Figure 5b when Q1 is on, and Q2 is off. Capacitor C5 is returned to ground through R9 and Q1. Therefore, C5 can develop a positive pulse to turn Q1 off. Q2 is off, so C6 is returned to -12 volts through R10 and R2. C6 cannot develop a positive pulse, and there is no need of one, because Q2 is already off. Note that any negative pulses developed are blocked by diodes, just as in the unsymmetrical inputs. If the signal into the "T" input is 0 volts and goes to -12 volts, a negative pulse is developed by both C5 and C6, but they are blocked by the diodes. The right side of C5 returns to 0 volts through R9 and Q1, but C6 maintains its relative charge of 0 volts, because Q2 is off. When the signal goes to 0 volts from -12 volts, a positive pulse will be developed by C5 and will forward bias D3. A positive pulse on the base of Q1 turns it off, and Q2 turns on. Now, C5 input is inhibited, and C6 is permissed by Q2 grounding RIO. The next positive transition of the input signal will put a positive pulse on the base of Q2 and Q2 will turn off and Q1 will turn on. Obviously, the "T" input will effect a transition either way, dependent upon the state of the flip-flop when the stage is triggered. Figure 5c combines the inputs of 5a and 5b. This is somewhat typical of the flip-flops in the EC-130.

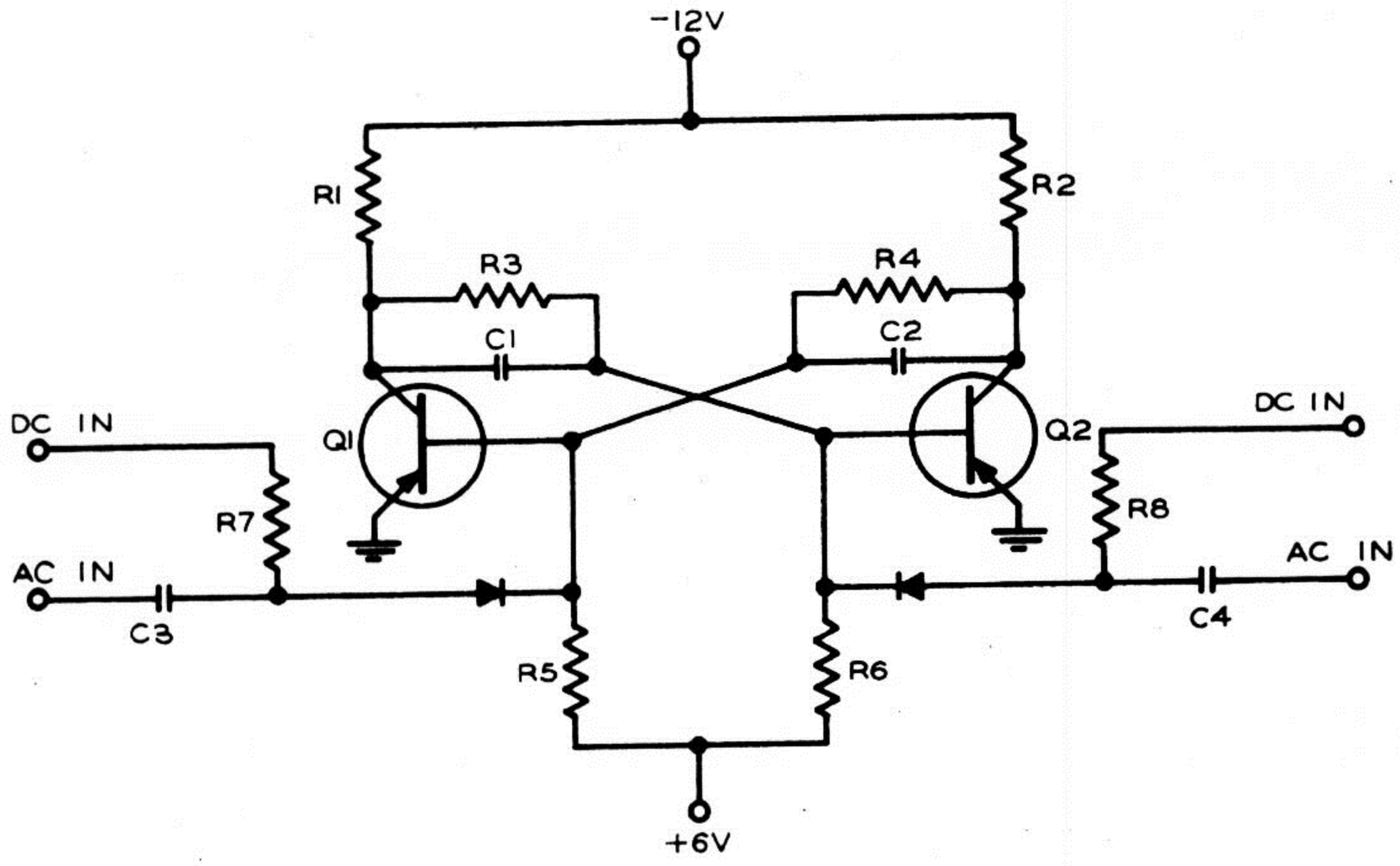


FIGURE 5a - Unsymmetrical Triggering

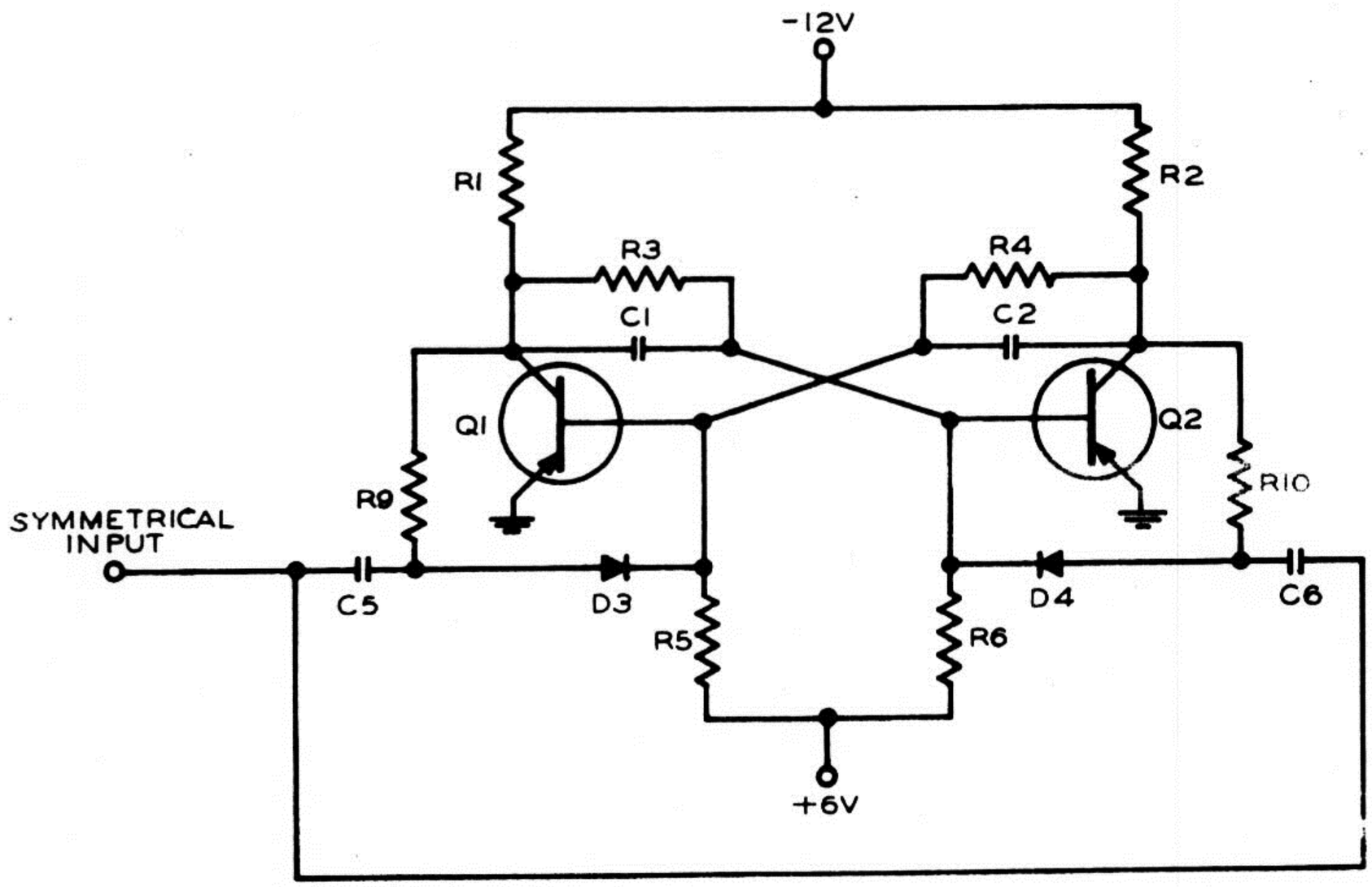


FIGURE 5b - Symmetrical Triggering

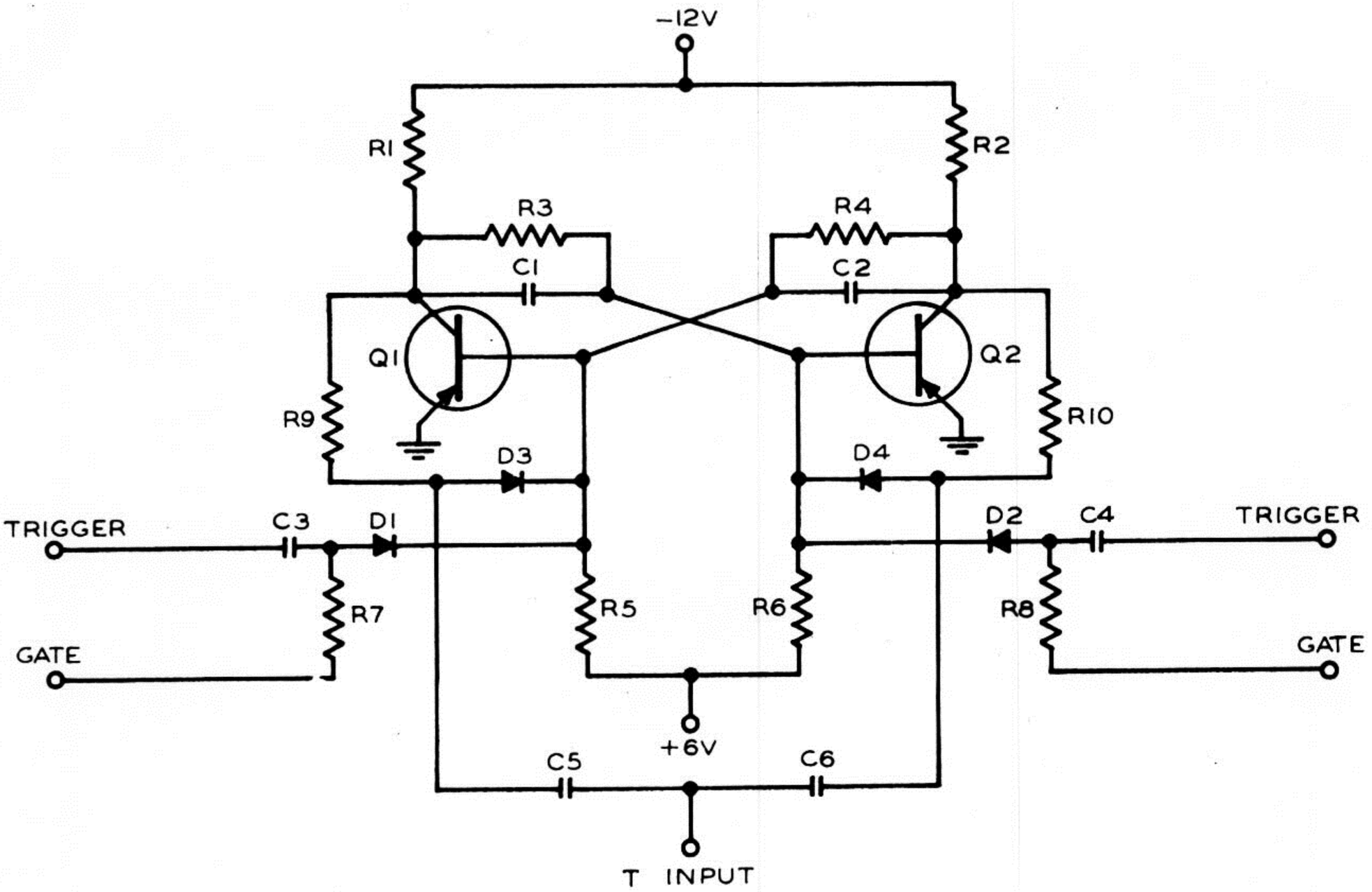
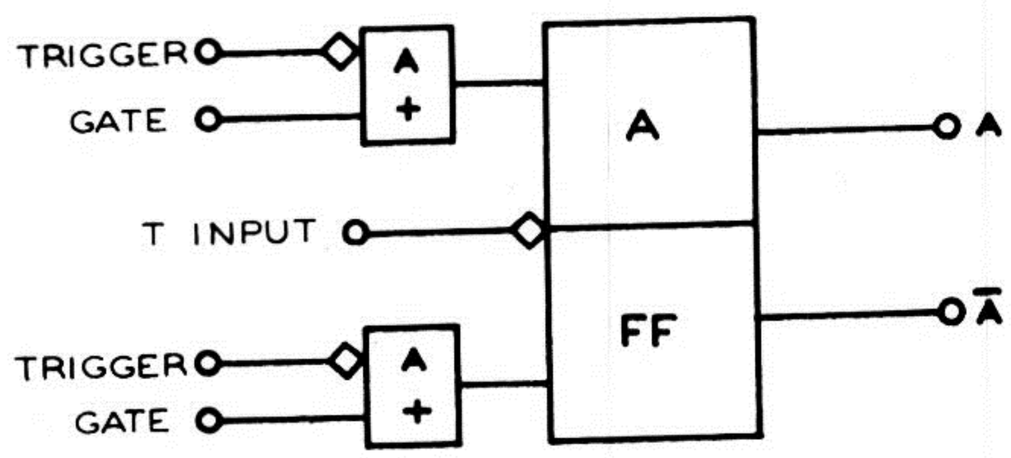


FIGURE 5c - A Typical EC/130 Flip-Flop



(Logic Symbol for Above Flip-Flop)