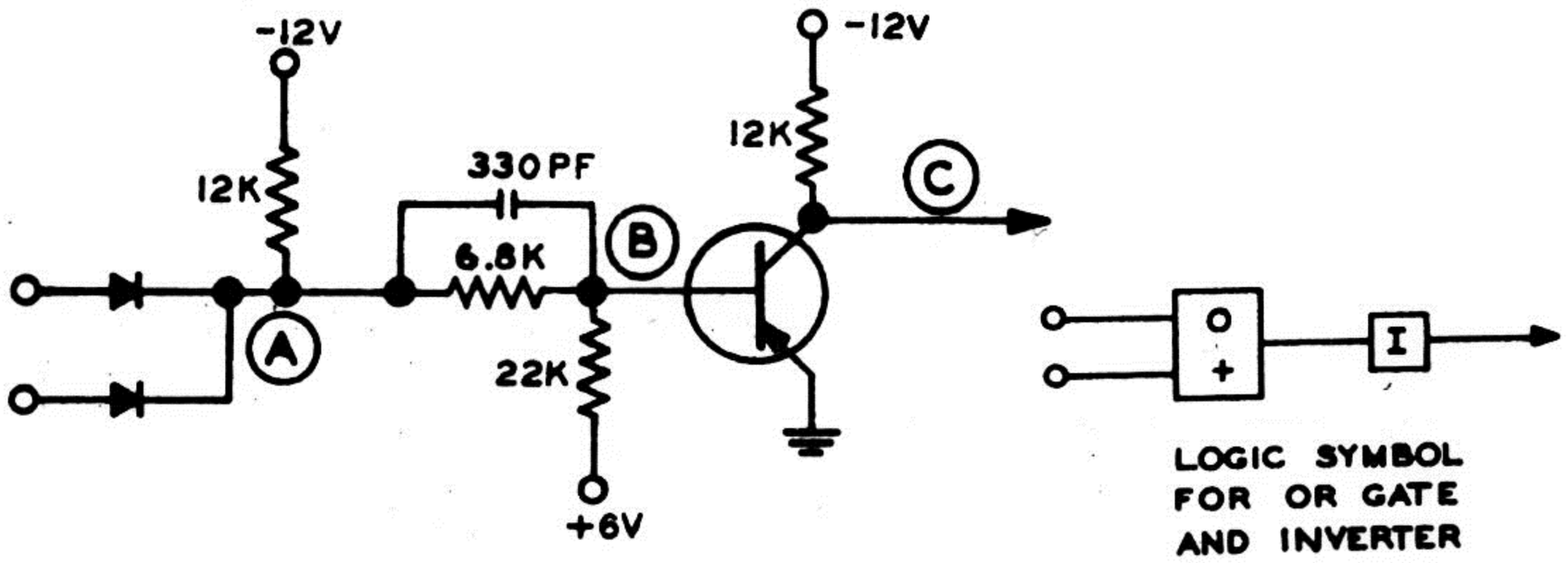
INVERTER

The inverter shown is classic for this machine. In some cases the component values change somewhat; in other cases the commutating capacitor has been omitted.



The operation remains the same. The inverter is often fed by a logic gate. In this example a positive OR gate is used. The first condition to be considered will be with -12 volt levels input to both diodes of the OR gate. Because point "A" is more positive than -12 volts, the diodes are back biased. Therefore, the OR gate acts as an open circuit and has no effect on the inverter circuit. The bias voltage for the transistor is determined by the voltage divider consisting of the 12K, 6.8K, and 22K resistors connected from -12 volts to +6 volts. If this voltage divider were not connected to the transistor at all, the voltage at point A would be -6.7 volts and at point B it would be -3.7 volts by Ohm's Law. When the base of the transistor is connected to point B, the base-emitter junction is forward biased, which puts point B at about -.2 volts. This level is usually considered to be 0 volts, but it is important to remember that

the base-emitter junction of the transistor is STILL forward biased. So, with the transistor connected to the voltage divider at point B, the voltage measurements will be different than those computed with the transistor base disconnected. Now, with the base-emitter junction forward biased, the effective voltage divider will be the 12K and the 6.8K connected from -12 volts to ground through the base-emitter junction. This will put point A at -4.35 volts and point B at -.2 volts (or, for practical purposes, at 0 volts) and the 330 P F capacitor will be charged to this value. With these conditions, the base current will be 12 volts divided by 18.8 x 10^3 ohms or .64 milliamps. The maximum collector current that can possibly flow is 12 volts divided by 12 x 10^3 ohms or 1 milliamp. A Beta of 2 is all that is necessary to drive the inverter stage into saturation and the Beta of 2N1305 is a minimum of 40, so it can be safely said that the transistor is in saturation. By definition, saturation means that the collector is clamped electrically to the emitter (within about .1 volts). But the emitter is tied to ground. Therefore, so is the collector. Therefore, the output, taken at point C, is 0 volts. The input (via the gate diodes in this example) is -12 volts. The inverter inverts.

Now the condition of the stage will be considered with either or both of the inputs to the OR gate at 0 volts. This will put point A at 0 volts (or thereabouts). Now the voltage divides. Under consideration is the 22K, and the 6.8K connected from +6 volts to 0 volts. This will put point A at 0 volts and point B at +1.25 volts. The 330 P F capacitor will be charged to this value.

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With point B at +1.25 volts, the base-emitter junction of the transistor is back biased, no base current flows, no collector current flows, and point C, the output, is at -12 volts. The input is 0 volts. The inverter still inverts.

The 330 pico-farad (micro-micro-farad) capacitor is a commutating, or speed-up, capacitor. Its purpose is to insure minimum rise and fall time. Consider the case above. With 0 volts input the capacitor is charged to +1.25 volts with 0 volts on the left plate. The transistor is cut off. Now when the input goes to -12 volts, the diodes are back biased, and point A goes to -4.35 volts. Capacitors oppose any change in charge, and this one is no exception. The capacitor was charged to +1.25 volts with the right plate (point B) at +1.25 volts. When the left plate (point A) goes to -4.35 volts, the capacitor maintains the charge between its plates that it originally had, that is, 1.25 volts. When point A changes 4.35 volts in a negative direction, point B MUST change 4.35 volts in a negative direction. Point B was +1.25 volts. +1.25 - 4.35 = -3.10V. But this is an instantaneous value and point B of the capacitor goes to -.2 volts very quickly through the emitter-base junction. This result in maximum emitter-base current at the beginning of the triggering signal. Therefore, collector current is maximum at the beginning of the triggering signal. This gives minimum rise time.

With the transistor on, the capacitor is charged to 4.35 volts, with -4.35 volts at point A, and about 0 volts at point B. When the input signal (either one) goes to 0 volts, the appropriate diode of the OR gate will be forward biased, putting point A at 0 volts. This is a change of 4.35 volts in a positive direction,

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so point B must also go 4.35 volts in a positive direction. This puts point B at 0+4.35 volts or+4.35 volts at the very beginning of this triggering signal. + 4.35 volts at point B turns the transistor off immediately. Point C goes from 0 volts to -12 volts in the minimum time possible.