EMITTER FOLLOWER

The load that a signal source sees is often a constantly fluctuating load, depending on the number and type of devices utilizing the signal at any given point in time. A heavy, fluctuating load can cause fluctuation in signal amplitude and loss of high frequency response. Additionally, if the load is capacitive, further reduction in high frequency response can be expected due to the integrating action of the load. If the signal source is a flip-flop, or oscillator, or an analog circuit, then the output impedence plays an important part in the circuit design, and a bouncing load, or even a steady low impedence load can unreasonably complicate design. These conditions are not desirable; their by-products are unreliability, complexity and reduced capability. Fortunately, there is a solution which permits a signal source to drive a heavy, fluctuating load without the source itself being unnecessarily loaded. This particular answer to the circuit designers' prayers is the emitter follower.

The emitter follower is the solid state equivalent of the familiar cathode follower in vacuum tube circuitry. Its functions are isolation, and impedence matching. Characteristics of the emitter follower are high input impedence and low output impedence. For example, consider the basic emitter follower in Figure 1. The output impedence is 1K (the output impedence equals the emitter resistor shunted by R_{CE}). But the input

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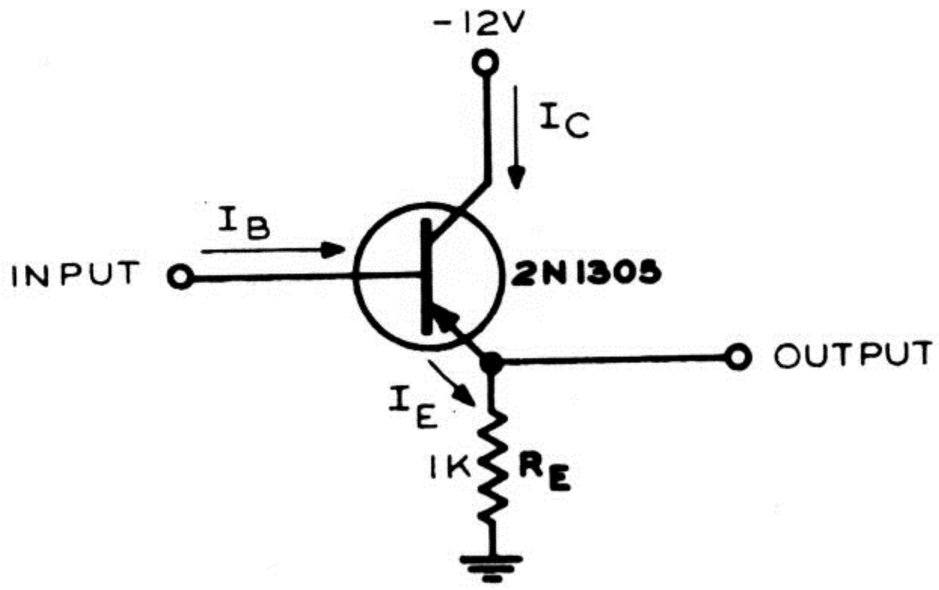

Figure 1

impedence is equal to the sum of the emitter-base junction resistance plus the emitter resistor, all multiplied by the quantity of beta plus one. Stated algebraically, $Z_{in} = (R_{be} + R_e) \times (B+1)$. If R_e is reasonably large, R_{be} (the emitter-base junction resistance) becomes inconsequential, and the formula becomes $Z_{in} = R_e (B+1)$. The minimum beta of a 2N1305 is 40, so $Z_{in} = 1 \times 10^3 \times 41$ or 41K.

Why does $Z_{in} = R_e(B+1)$? Mere acceptance of the formula is not as good as understanding WHY the formula is true. First, assume that the input signal is -5 volts D.C., and that beta is 100. Enough emitter current will flow to create a 5 volt drop across R_e (ignoring the .1 or .2 volt drop across the emitter base junction). The current necessary to cause 5 volts to drop across 1K is 5 ma ($I = \frac{E}{R}$). The emitter current is 100 parts collector current, and 1 part base current. Stated differently, $I_b = \frac{I_e}{B+1}$, so $I_b = \frac{5 \times 10^{-3}}{101} = 49.5$ u amps. Now

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stop to think for a moment! If 5 volts applied from the base of the transistor to ground causes 49.5 u amps of base current to flow, what MUST the effective resistance be? Resistance equals voltage divided by current. $R = \frac{5}{49.5 \times 10^{-6}} = 101K$. Hence the input impedence equals R_e times beta plus one! Amen.

Now, about isolation. To say that an emitter follower isolates the output from the input implies that a change in the output characteristics has no effect upon the input. This is not technically true, and Figure 2 will be used to show why this is not TECHNICALLY true. Note the similiarity

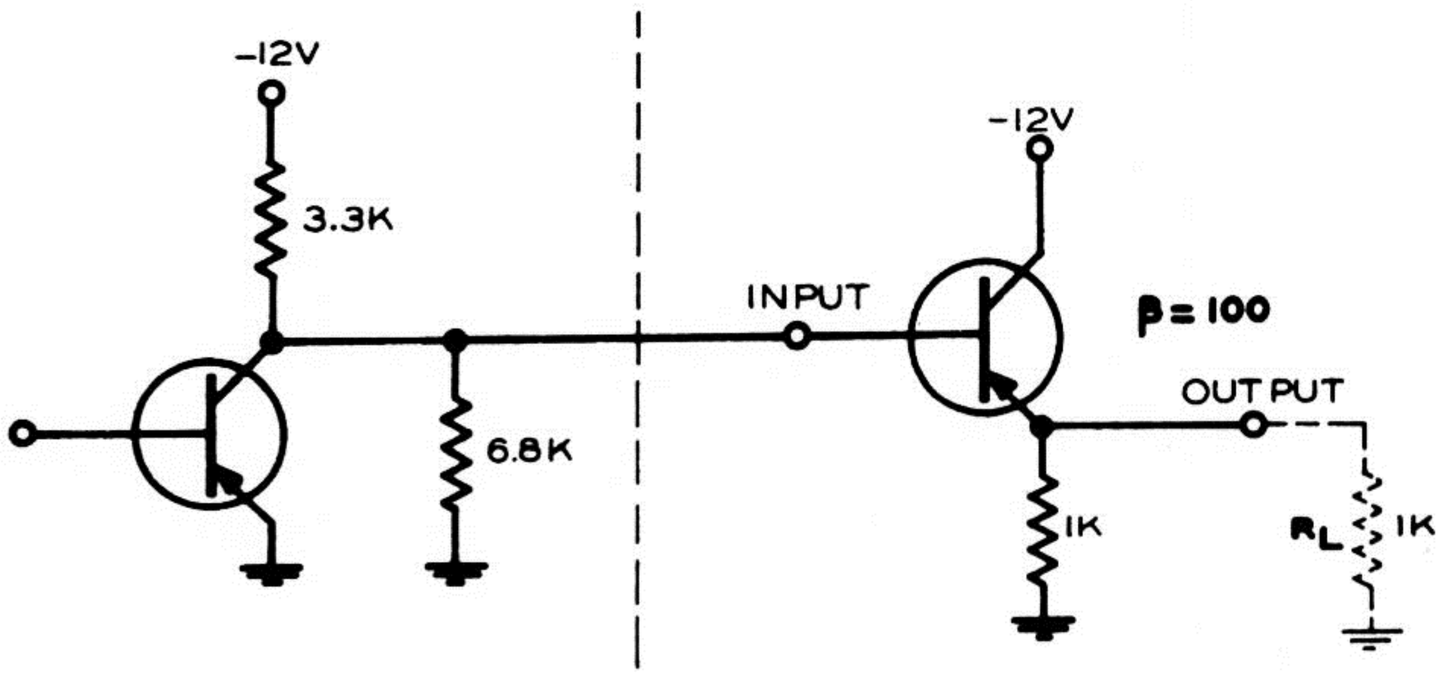

Figure 2

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of Figure 2 to Figure 1. The only difference is a realistic input signal source. The emitter follower input impedence is still 101K. But this 101K effective resistance is paralleled by the 6.8K resistor to ground. The equivalent resistance of this parallel circuit is 6.25K. The 6.25K resistance forms a voltage divider with the 3.3K resistor, so when Q1 is off, -7.85 volts is applied to the base of the emitter follower. Under no-load conditions, the emitter current is about 7.75 ma. If suddenly a 1K load is connected to the output, emitter current must increase to 15.5 ma. The question is, will this drastic change affect the input signal amplitude? If there is no change in the input signal amplitude, then isolation is achieved, but if the signal amplitude decreases, then there is poor isolation.

With a 1K load connected in parallel with Re, the effective emitter resistance is 500Ω. The emitter follower input impedence is (B+1) times 500 ohms, or 50K. With 50K in parallel with the 6.8K resistor instead of 100K as before, the equivalent resistance is 6.1K and the signal level is -7.8 volts. Result: doubling the current requirement of the emitter follower output circuitry resulted in a change in signal amplitude of .05 volts. So,a change in the output requirements of the emitter follower does have some effect upon the input signal, but under normal conditions this effect is so small that it can be ignored, and good isolation is considered to be achieved. (Actually, with the equipment Friden employees will be using, it is practically impossible to tell the difference between -7.85

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volts and -7.8 volts anyway, and component tolerences allow more change than that.) For all practical purposes the emitter follower provides good isolation, although technically there is some interaction. (It will be left to the reader to determine what the effect will be on the input signal and the transistor if the 1K resistor is shorted.)

When the emitter follower is actually put into use in a particular circuit, other considerations arise and must be dealt with. Take for example, a typical application where an emitter follower drives 4 diode gates. This circuit is shown in Figure 3 using the "typical" emitter follower just analyzed. Note that of gates #1, #2, #3, #4, only the diodes

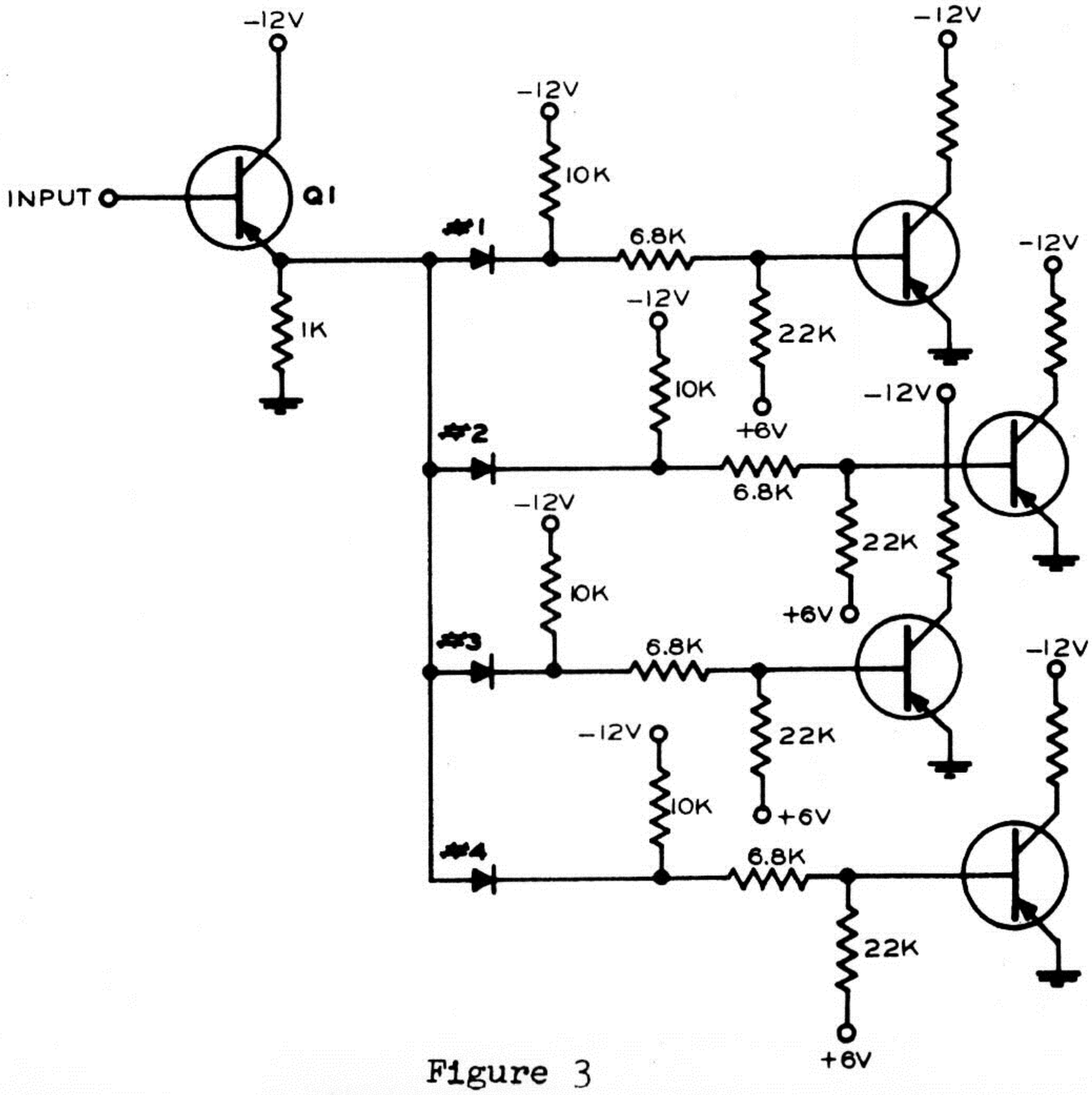

Figure 3

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that Q1 are driving are shown. This is done for simplicity, because only these diodes are of concern in looking at the application of the emitter follower. When the input of Q1 is at -8.1 volts, the output of Q1 is at -8 volts, and each of the diodes is back biased. The four inverters are on, and there is about -4.9 volts on the cathodes of the diodes.

When the input to Q1 goes to 0 volts, Q1 turns off and the output should go to 0 volts also. But now, those 4 diodes are forward biased, and the 1K resistor is connected to -12 volts through 4 10K resistors in parallel. The equivalent resistance of 4 10K resistors in parallel is 2.5K. This equivalent resistance is in series with the 10K resistors to form a voltage divider as shown in Figure 4. The voltage at point A is,

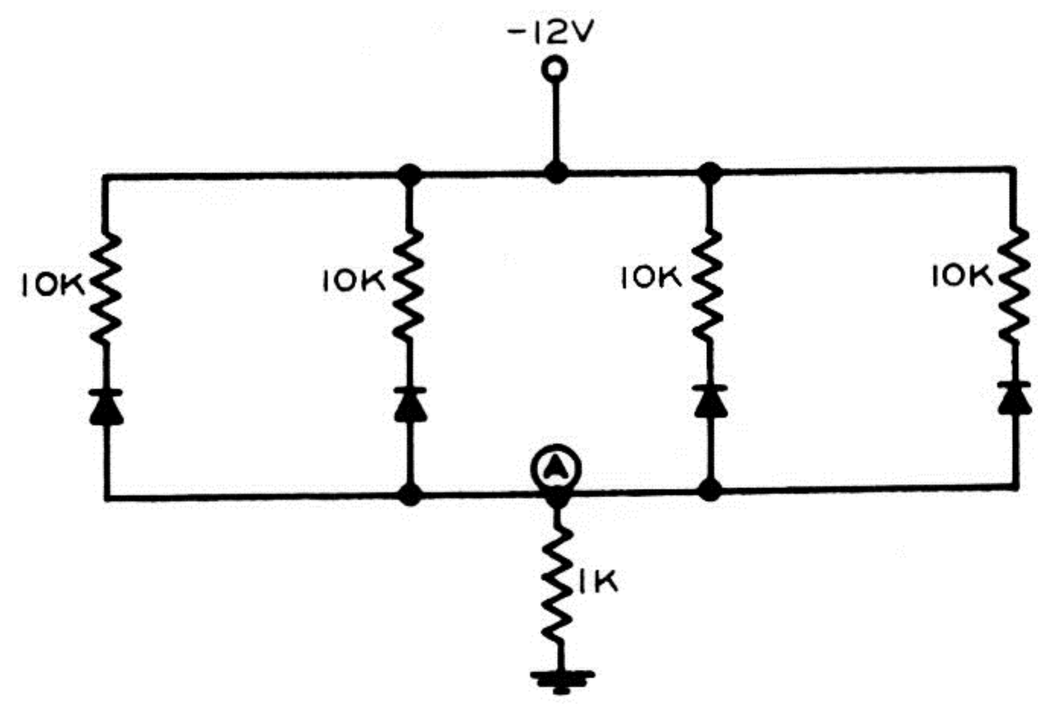

Figure 4

therefore, $\frac{-12}{2500+1000}$ x 1000 = -3.4 volts. With -3.4 volts on the cathodes of the diodes (they're forward biased), the bases of the inverters are trying to go to -1.1 volts which

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means that the inverters are still on, although when the emitter follower turned off, the inverters should have turned off also. Alas, they didn't!

The immediate thought that comes to mind is to alter the value of the resistors involved, but if the 10K bias resistors are increased significantly, the 6.8K and 22K resistors must also be increased a proportional amount which decreases base current in the inverters and decreases the reliability of the circuit. If the 1K resistor on the emitter follower is decreased, the power dissipation in Q1 (Figure 3) goes up, and so do the power requirements of the power supply. These are not solutions; they are merely a different set of problems.

One solution to the problem is to make Q1 an NPN equivalent of the 2N1305. This is the 2N1304, and the circuit is shown in Figure 5. Compare this with Figure 3. Note that in Figure 5 only one diode gate is used with a 2.5K to -12 volts. This is electrically equal in loading to the four gates with their 10K resistors to -12 volts. Now, when the input to Q1 is -8.1 volts, the output will be -8 volts as before and the diode will be back biased. When the input goes to 0 volts, Q1 is in saturation, and the emitter is clamped to the collector, but the collector is grounded! Now the only resistance between ground and -12 volts is the 2.5K resistor (or the 4 10K resistors in parallel). The cathode of the diode is clamped firmly to ground except for about .4 volts dropped across the junctions of the transistor and the diode. Problem solved!!

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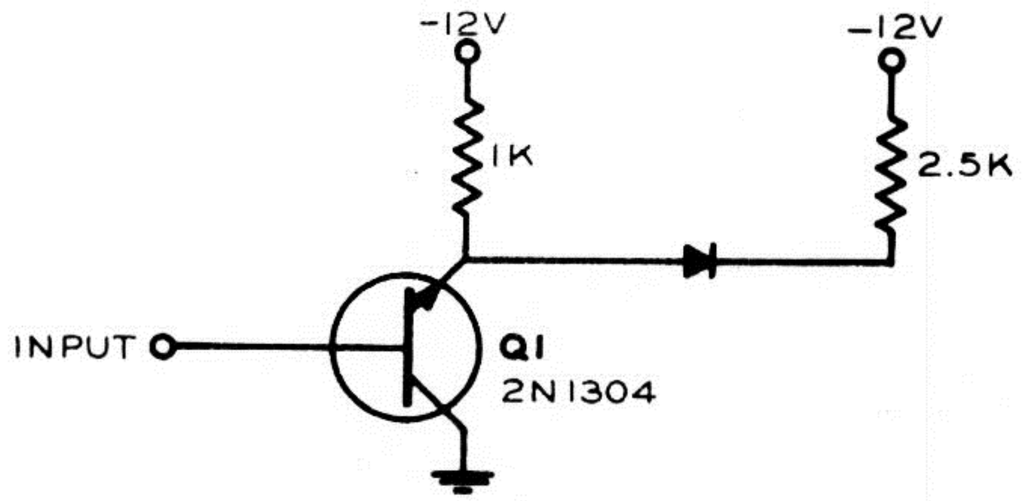

Figure 5

Using an NPN emitter follower is not to be considered a cure-all for emitter follower problems. In the problem just discussed, it was desired to have the output clamped firmly to ground during logic 1; since there was no heavy load during logic 0 (output low), that portion of the waveform could be ignored. What if the loading is reversed, that is, a heavy load at logic 0, and no load, or a light load during logic 1? Then a PNP emitter follower comes into its own. Look at Figure 6. Here, the loading is to ground instead of to -12 volts. If an NPN transistor had been used instead of a PNP, the maximum negative voltage the output signal could have attained is -4 volts. (It is left to the reader to discover why.)

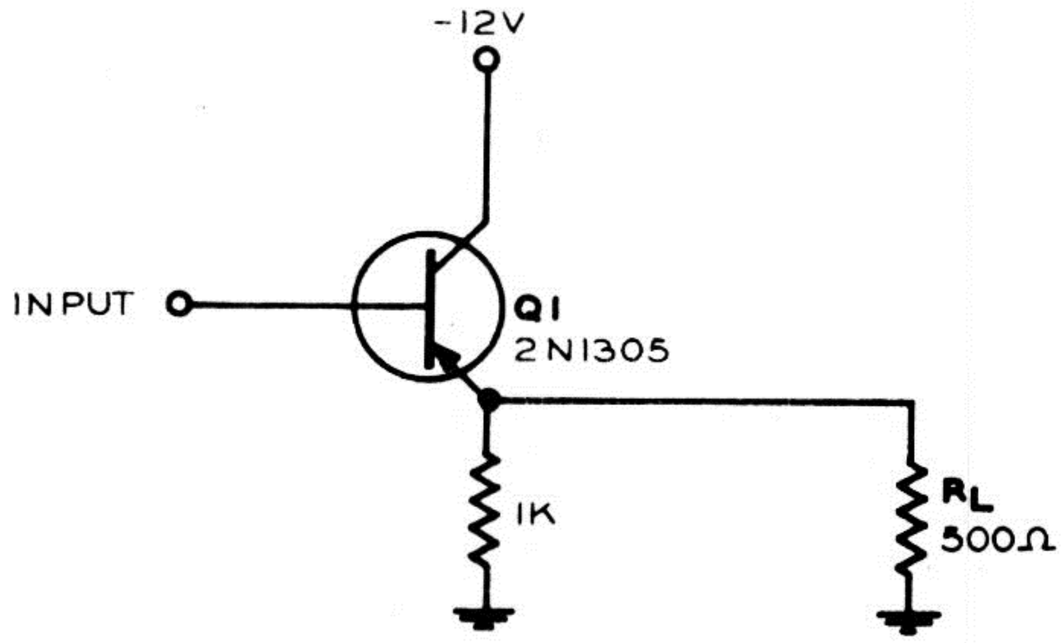

Figure 6

Another factor to consider is the type of loading. Thus far only resistive loading has been considered. What if the load is capacitive as, for example, it would be if the output were used to trigger a couple of flip-flops (see article on flip-flops). Figure 7 shows a P.N.P. emitter follower and the trigger circuit of two flip-flops. Consider first that the output of Q1 is -8 volts and that C1 and C2 are charged to 8 volts. When the input goes to 0 volts, Q1 will turn off and one would expect to see a sharp, fast, over-compensated, positive pulse on the anode of the diodes. But instead, C1 and C2 act like any two capacitors in parallel would, and begin to DISCHARGE through the 1K emitter resistor. Two 500PF capacitors in parallel equal 1000PF. One time constant of 1K and 1000PF equals 1 u sec, and it will take 5 time constants, or 5 u sec for the left sides of the capacitors to reach 0 volts. This can hardly be considered

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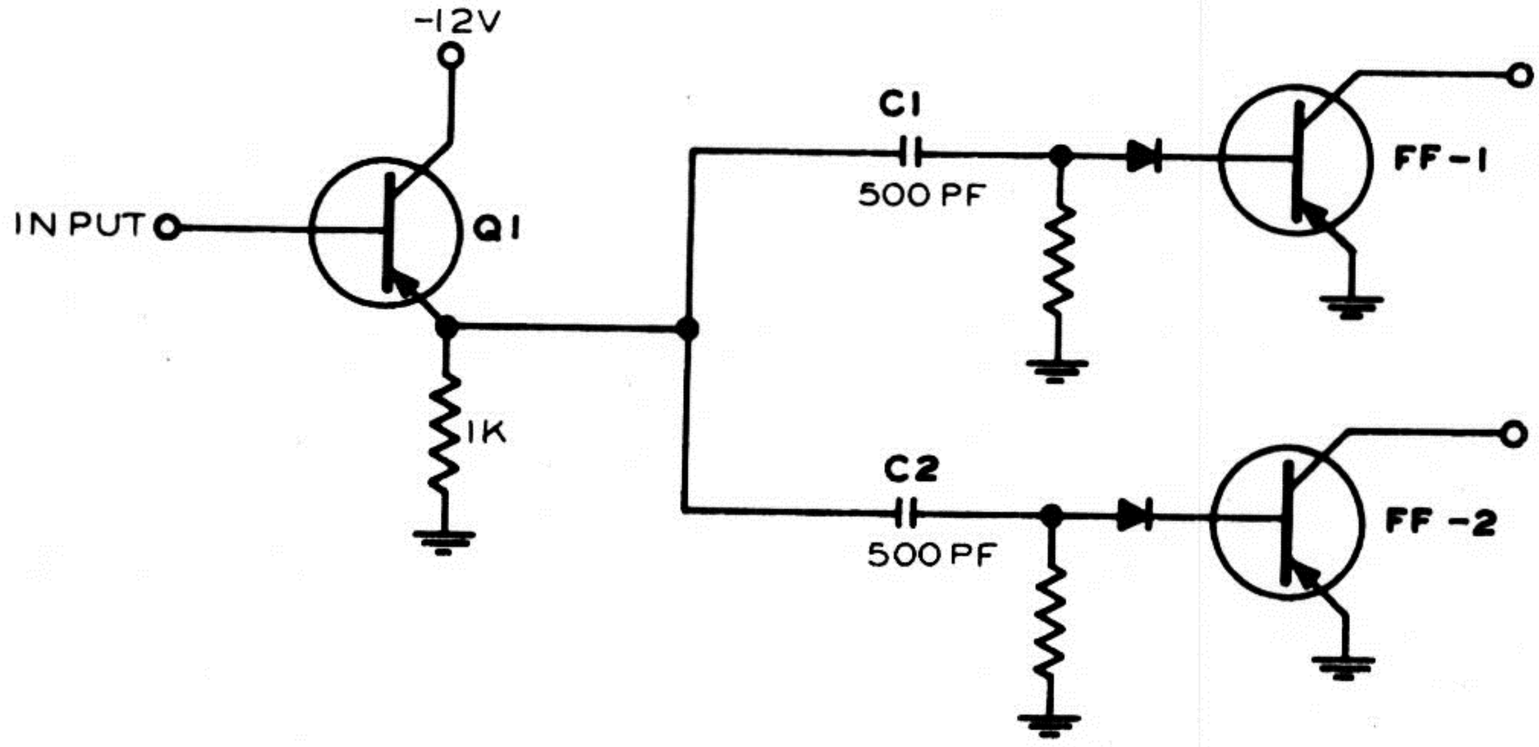

Figure 7

a fast rise time! If Q1 is made an NPN emitter follower with the collector grounded, then when 0 volts is put on the base, the emitter immediately goes to 0 volts, driving the right side of the capacitors to +8 volts immediately and this will flip the flip-flops very quickly.

In short the design of a transistor must be contingent upon the desired input and output impedences, which part of the signal will be considered significant (that is positive or negative) and the type of loading.